

# Compal Confidential

## VSKAA Schematics Document

Haswell with DDR3L + Lynx Point PCH

nVIDIA N14P-GV2 (Dual Rank)

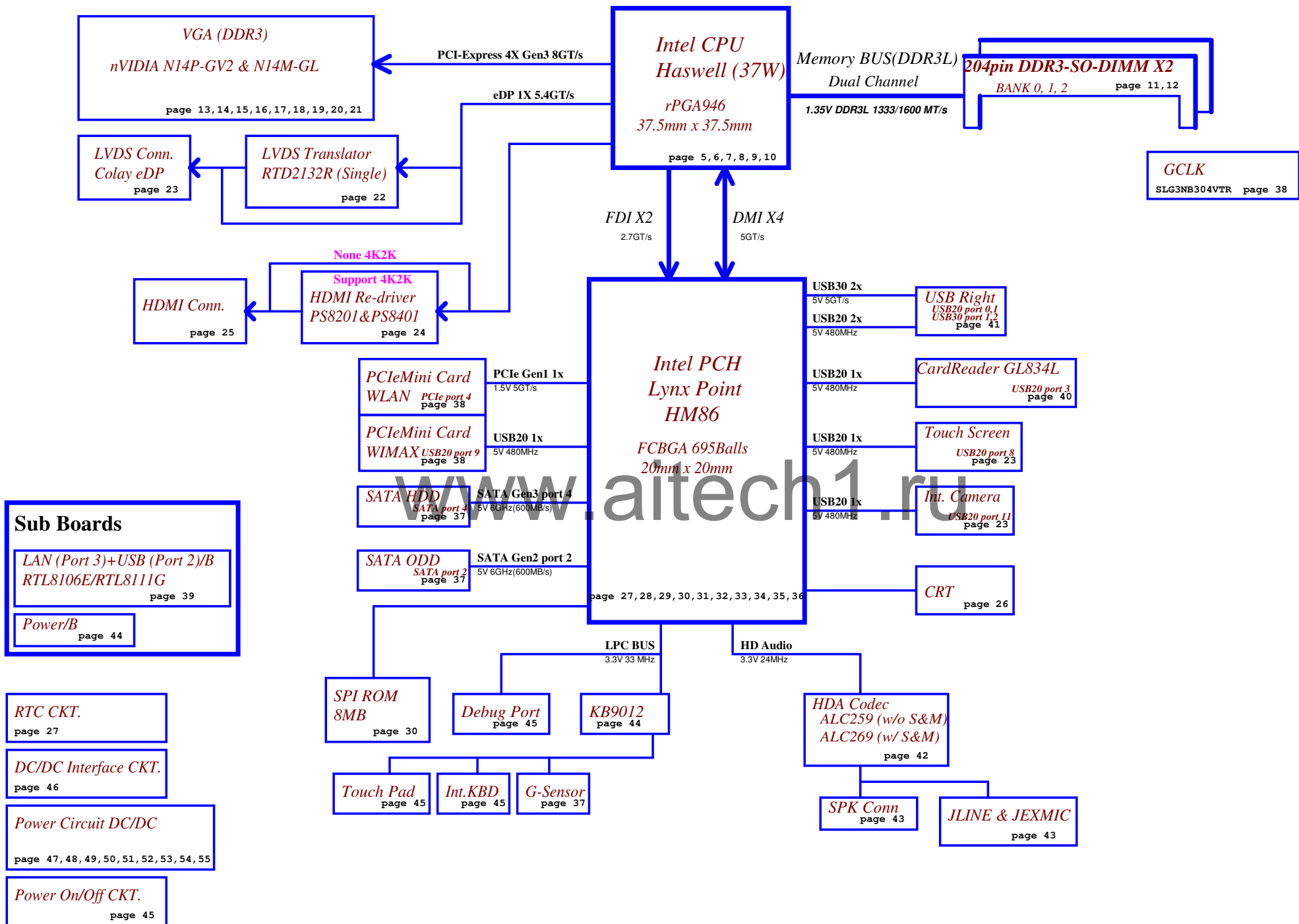
nVIDIA N14M-GL

# LA-9866P REV 1.0 Schematic

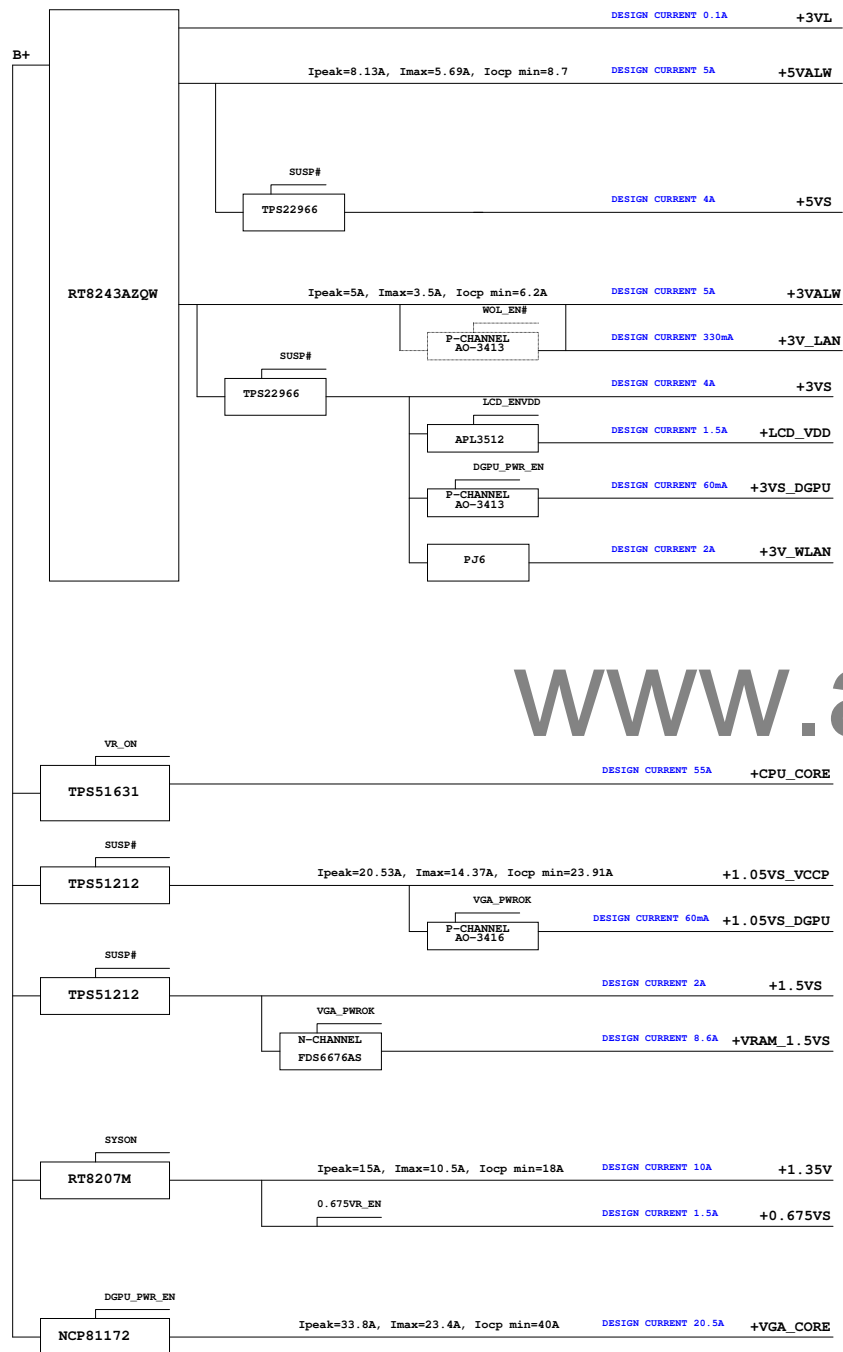
Intel Processor (Haswell) / PCH(Lynx Point)

2013-04-28 Rev 1.0

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Voltage Rails ( O MEANS ON X MEANS OFF )						
power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.35V	+5VS +3VS +1.8VS +1.5VS +CPU_CORE +VGA_CORE +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address			
Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address				EC SM Bus2 Address			
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b	+3VS	NVIDIA GPU	9E H	1001 1010 b
Power	Device	HEX	Address				

Platform	SKU	CPU	PCH	VGA
Chief River		Ivy Bridge i3 (CPUI3@) Ivy Bridge i5 (CPUI5@)	HM77C1 (HM77@) HM77C1_R1 (HM77R1@) HM77C1_R3 (HM77R3@)	nVIDIA N13P-GL (N13PGL@)

BTO Option Table

Function	SKU	MIC	LAN			
description						
explain						
BTO						

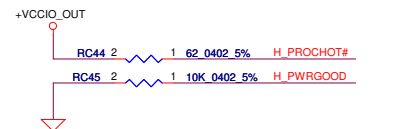
Function						
description						
explain						
BTO						

Function						
description						
explain						
BTO						

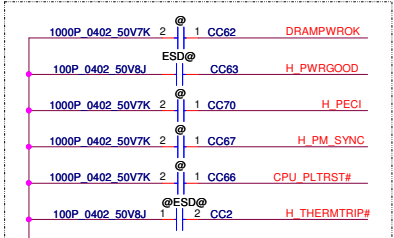
Function		
description		
explain		
BTO		

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

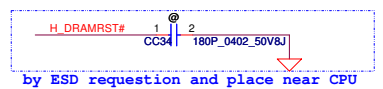
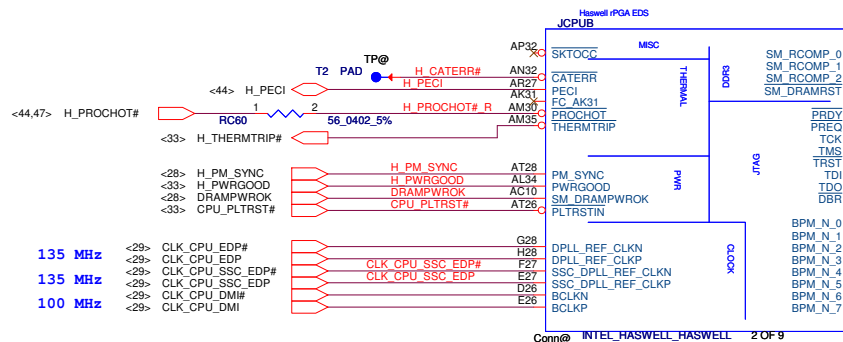




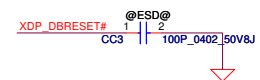
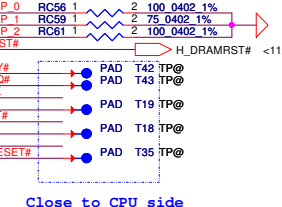
If no use eDP, please stuff them.



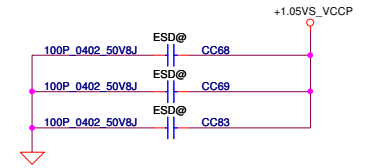
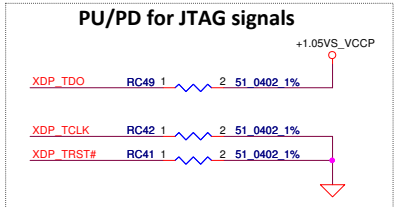
Please place near JCPU



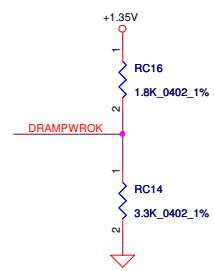
DDR3 Compensation CAD Note:  
Trace width=12~15 mil, Spacing=20 mils  
Max trace length= 500 mil



### XDP Connector reserve test point

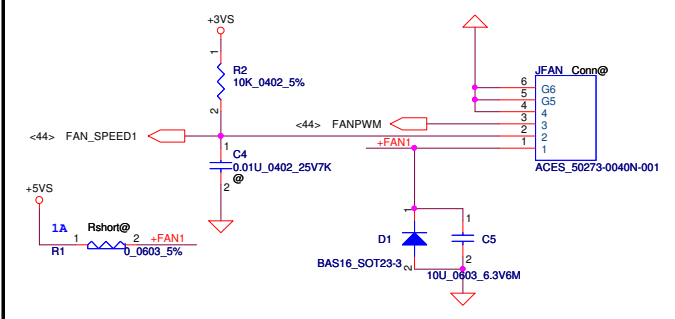


### SM\_DRAMPWROK for nonsupport Deep S3

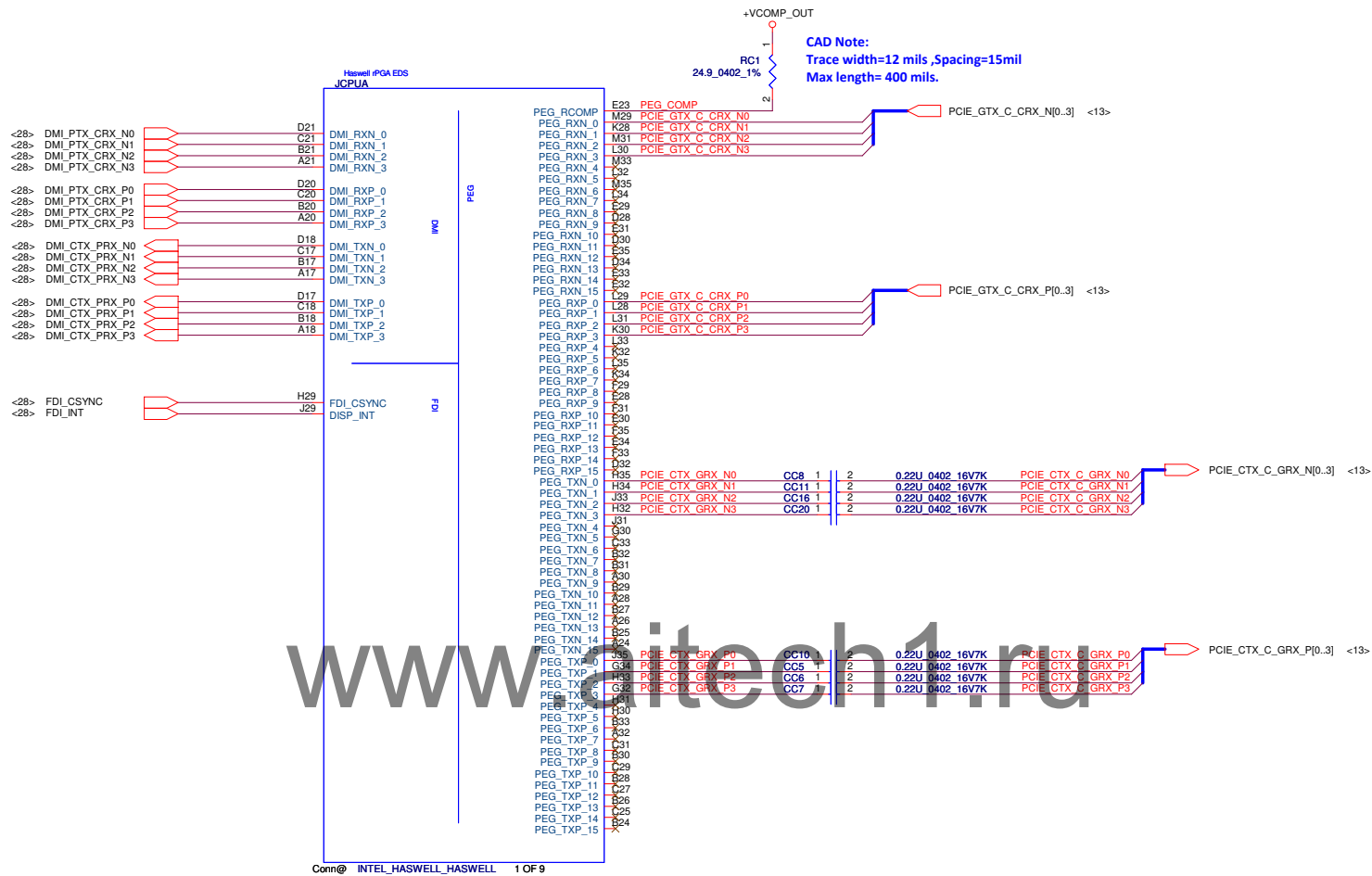


### Buffered Rest to CPU

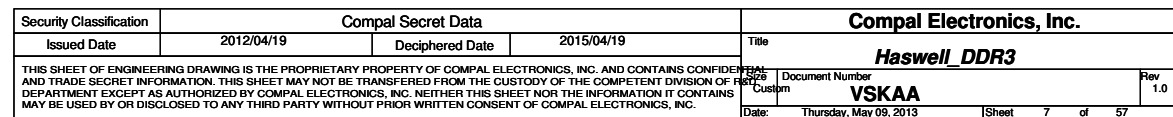
### FAN Control Circuit

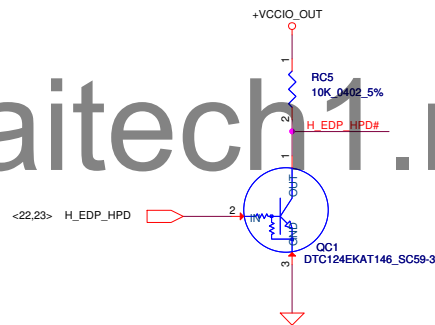
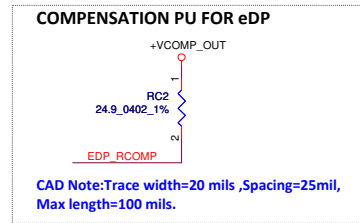
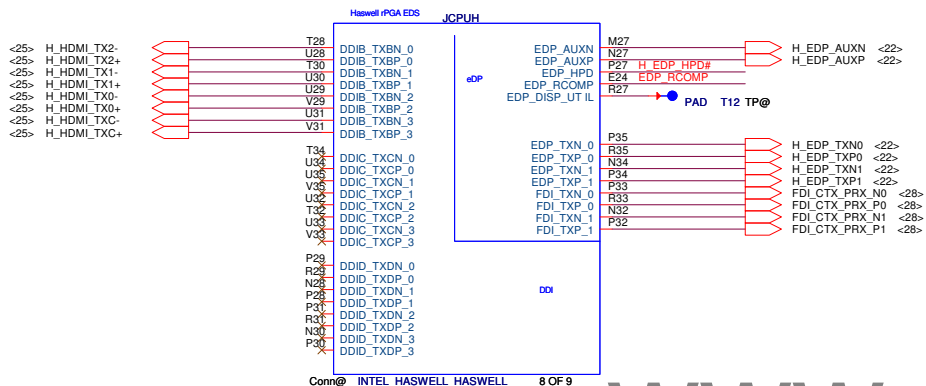


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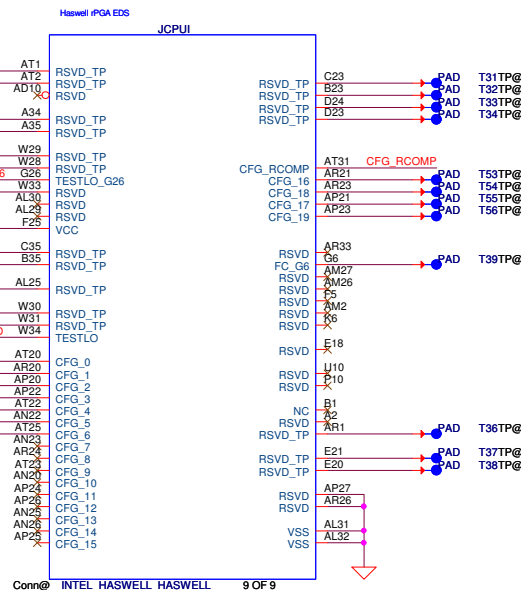


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1 CPU TESTLO G26  
2 CPU TESTLO  
1 CPU TESTLO  
2 CPU TESTLO  
1 CPU TESTLO  
2 CPU TESTLO



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## CFG Straps for Processor

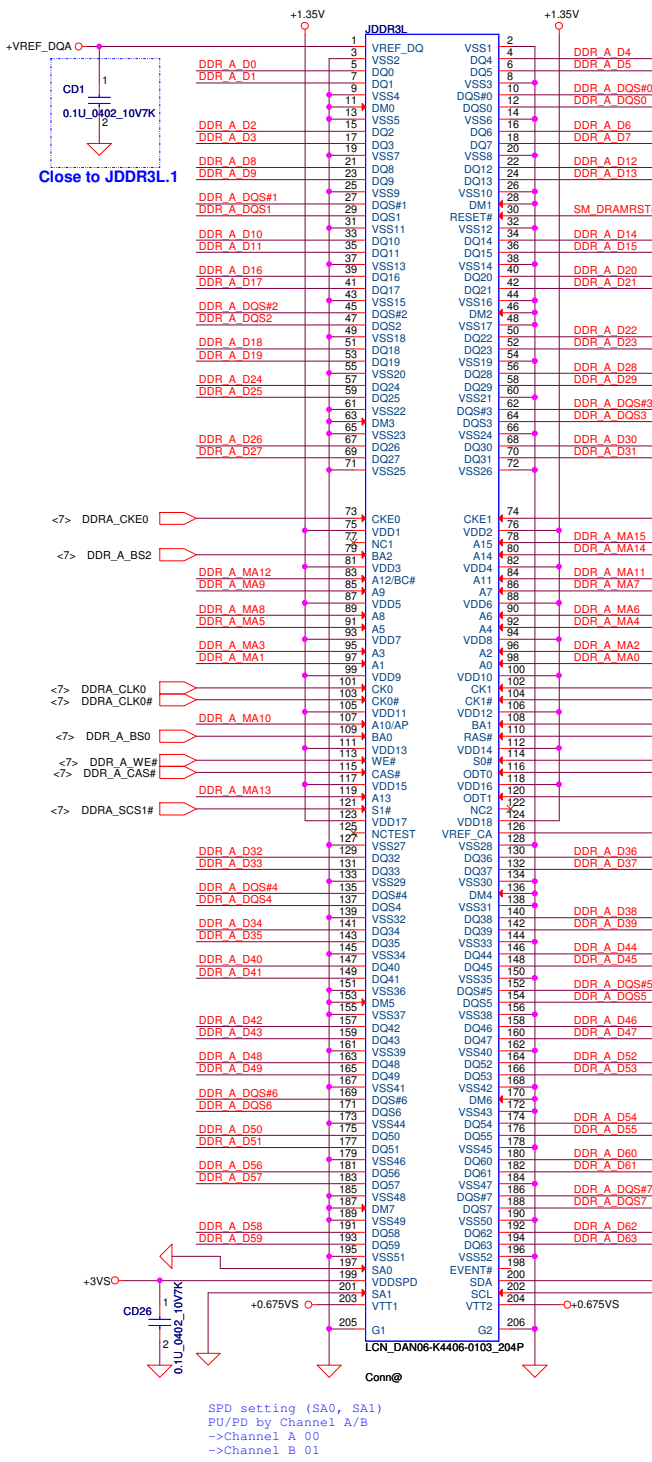
(CFG[17:0] internal pull high 5~15K to VCCIO)

CFG2	
PEG Static Lane Reversal - CFG2 is for the 16x	
★ 1: Normal Operation; Lane # definition matches socket pin map definition	
0: Lane Reversed	

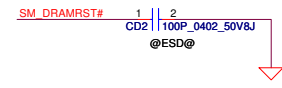
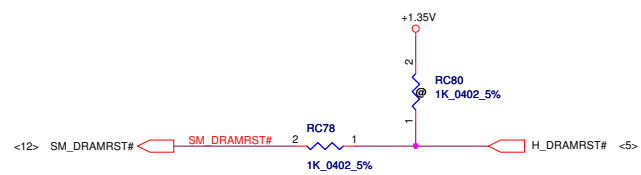
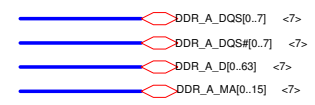
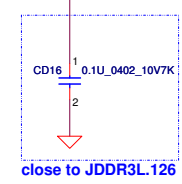
CFG4	
Embedded Display Port Presence Strap	
1 : Disabled; No Physical Display Port attached to Embedded Display Port	
★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port	

CFG6:5	
PCIE Port Bifurcation Straps	
★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled	
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled	
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)	
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled	

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DDR3 SO-DIMM A  
Reverse Type  
H=4.0mm

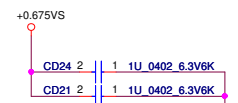
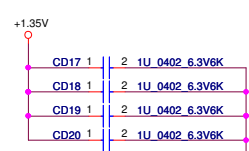
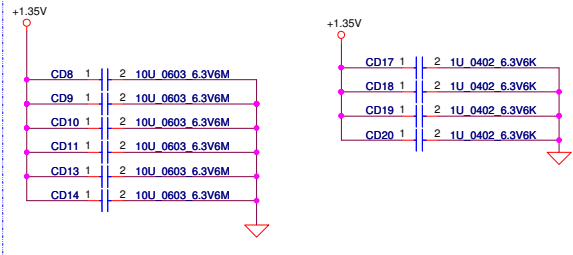


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Layout Note:  
Place near JDDR3L

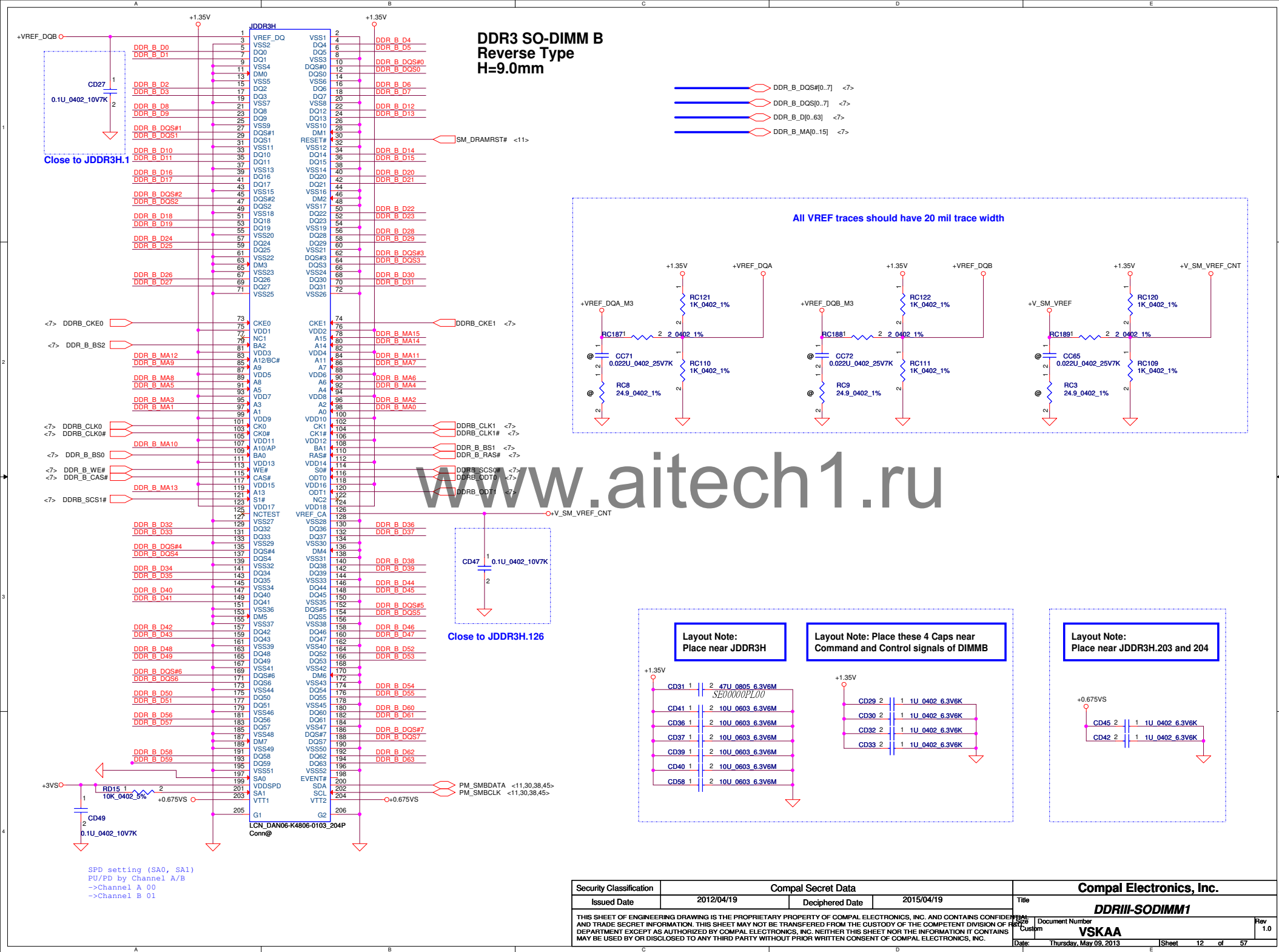
Layout Note: Place these 4 Caps near  
Command and Control signals of DIMMA

Layout Note:  
Place near JDDR3L.203 and 204



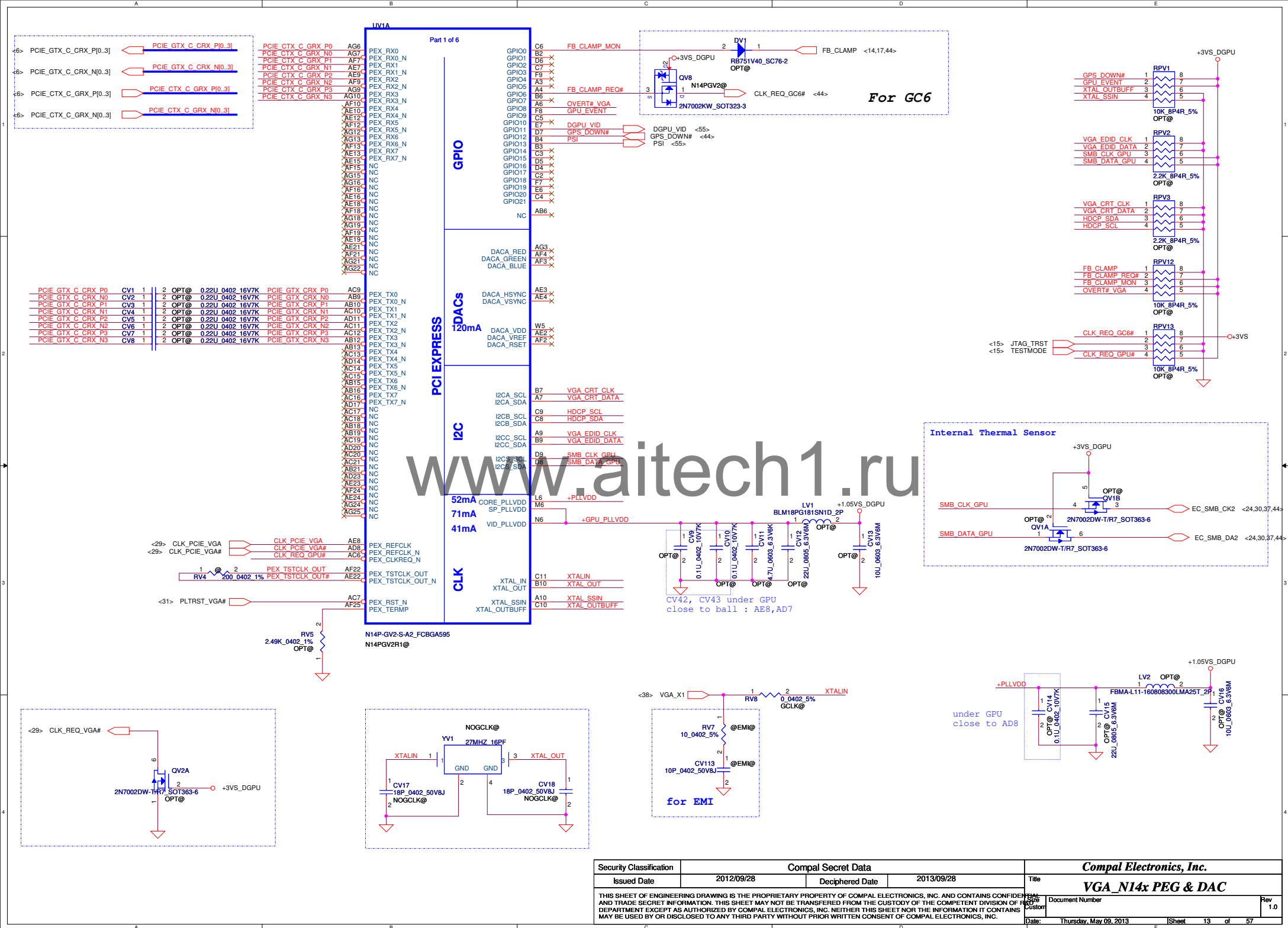
SPD setting (SA0, SA1)  
PU/PD by Channel A/B  
->Channel A 00  
->Channel B 01

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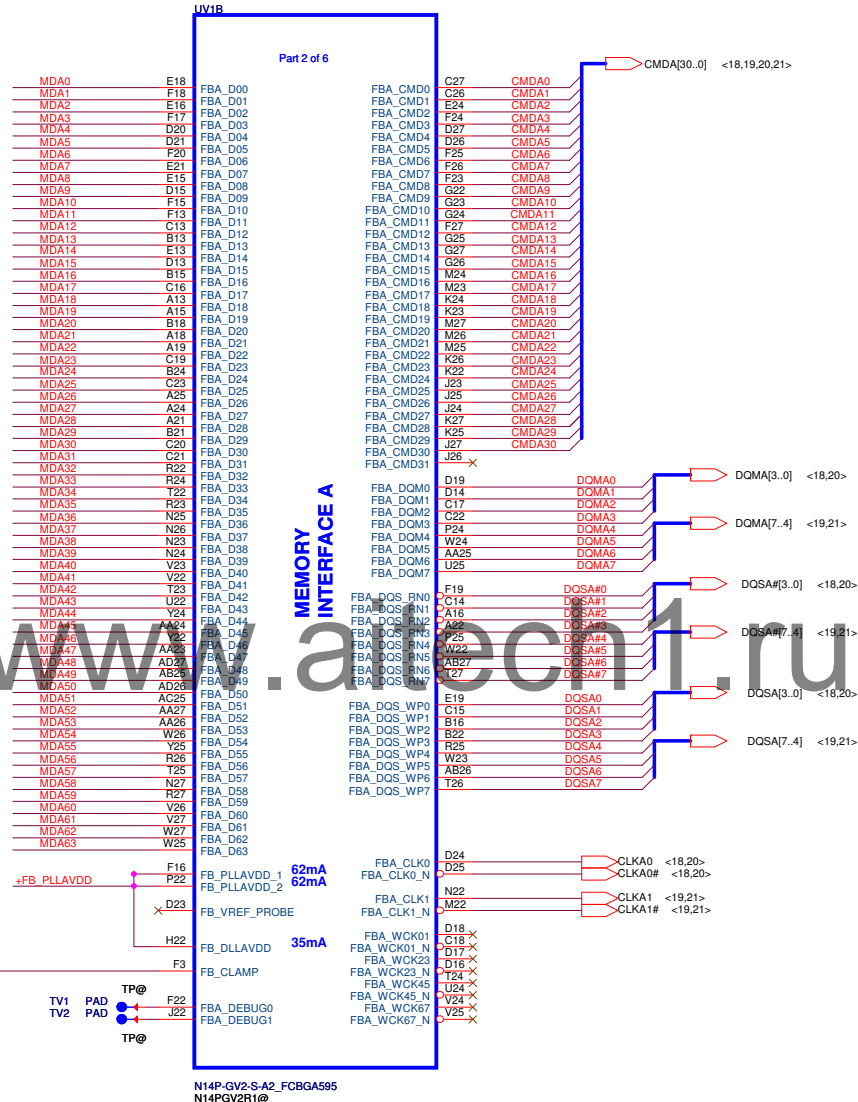
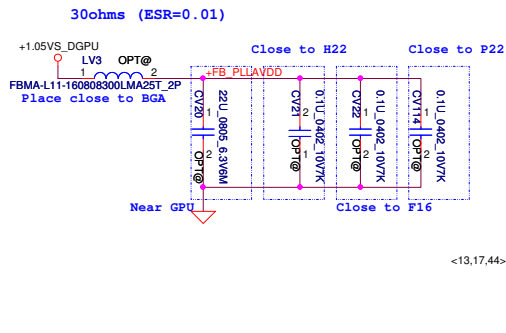
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				Part Number <b>VSKAA</b>			
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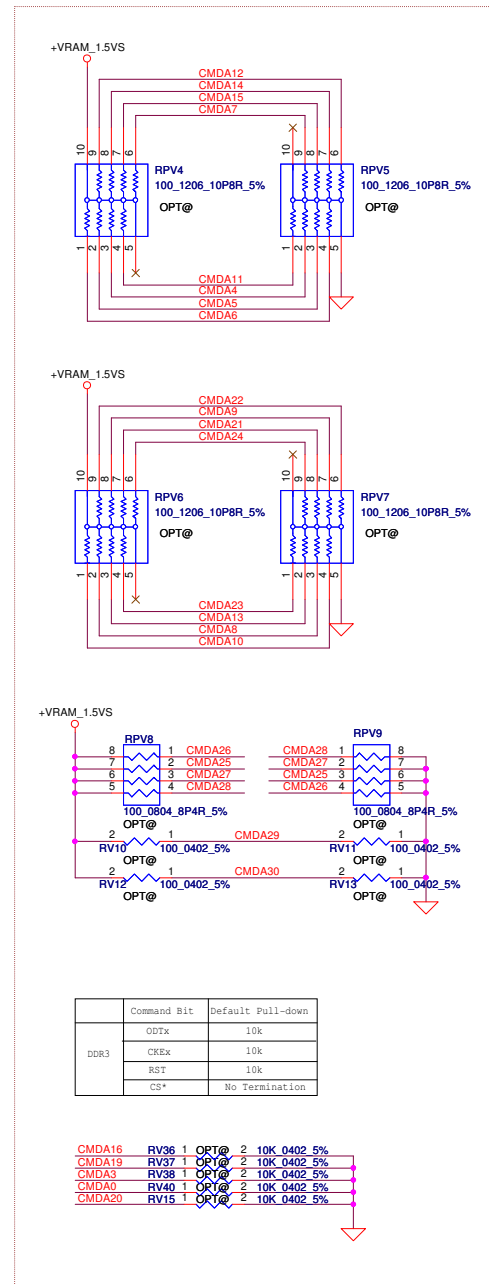


# VRAM Interface

<18,20> MDA[15..0]  MDA[15..0]  
 <18,20> MDA[31..16]  MDA[31..16]  
 <19,21> MDA[47..32]  MDA[47..32]  
 <19,21> MDA[63..48]  MDA[63..48]

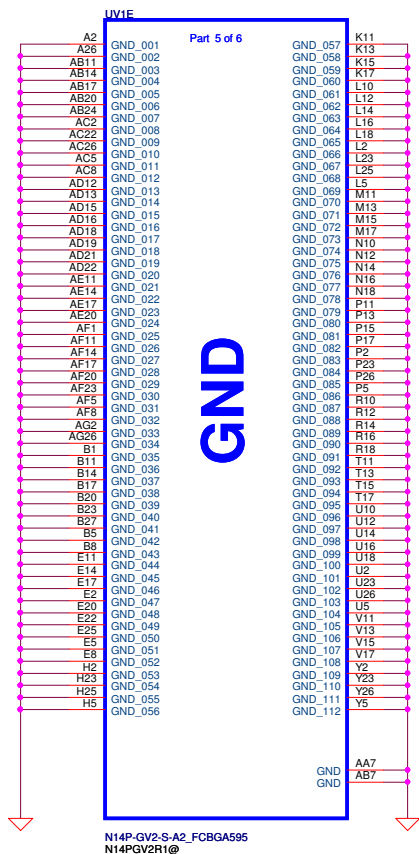


Place close to the first T point

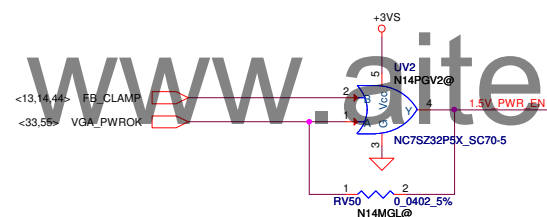




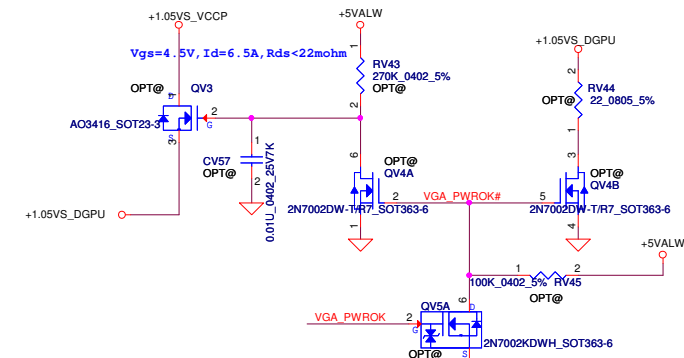




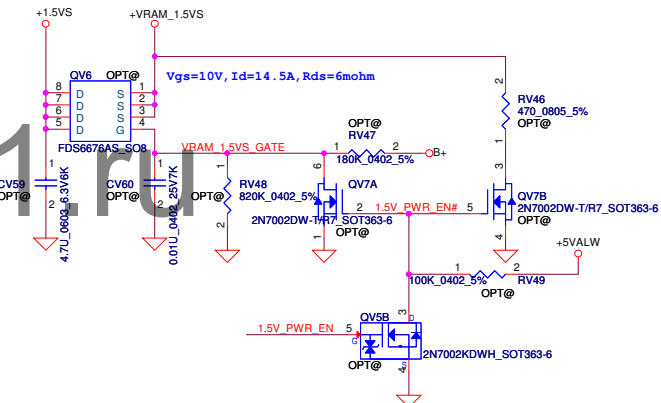
For GC6



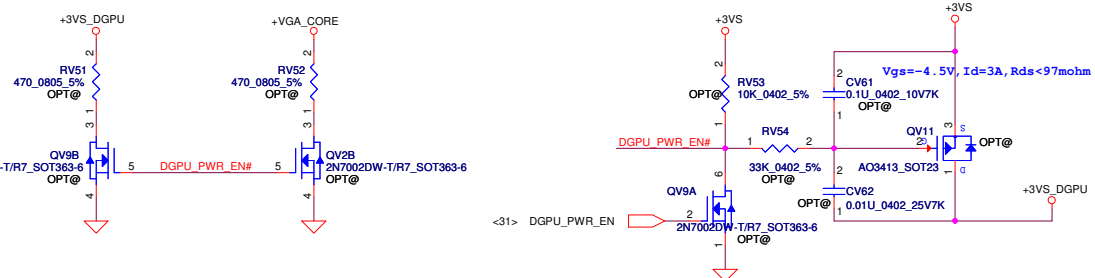
## +1.05VS\_VCCP to +1.05VS\_DGPU



## +1.5V to +VRAM\_1.5VS

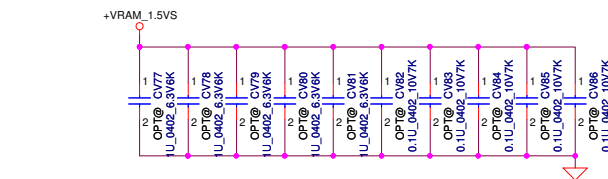
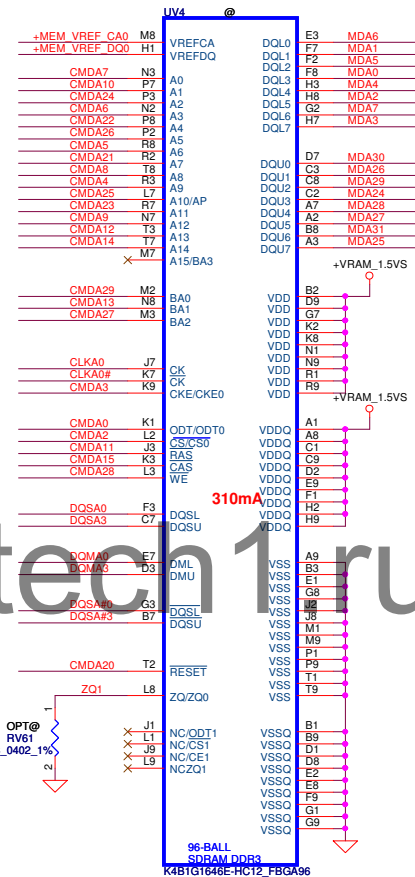
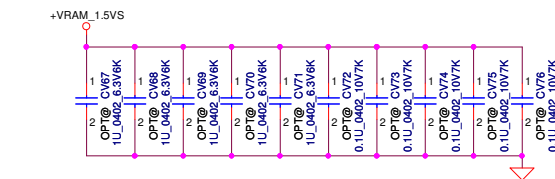
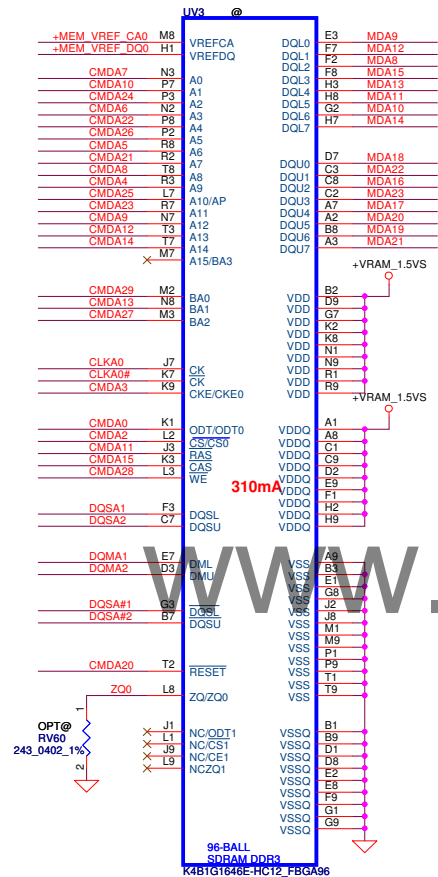
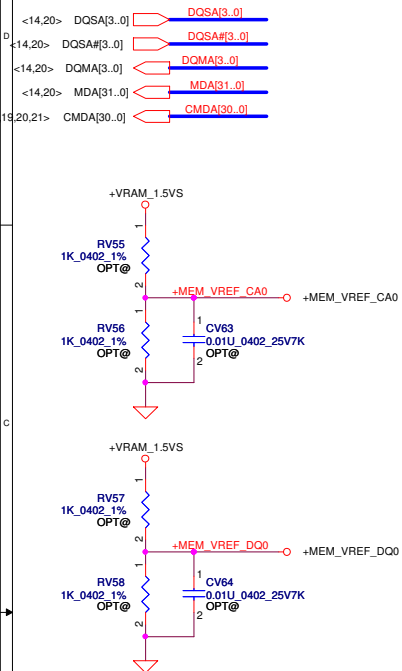


## +3VS to +3VS\_DGPU

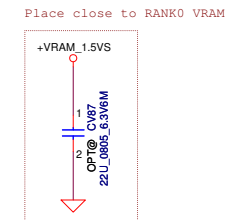
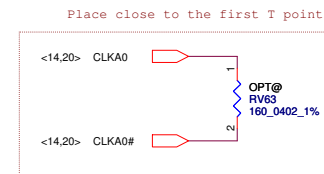


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## VRAM DDR3 Chips

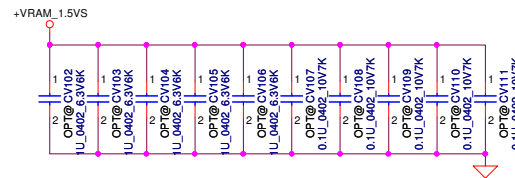
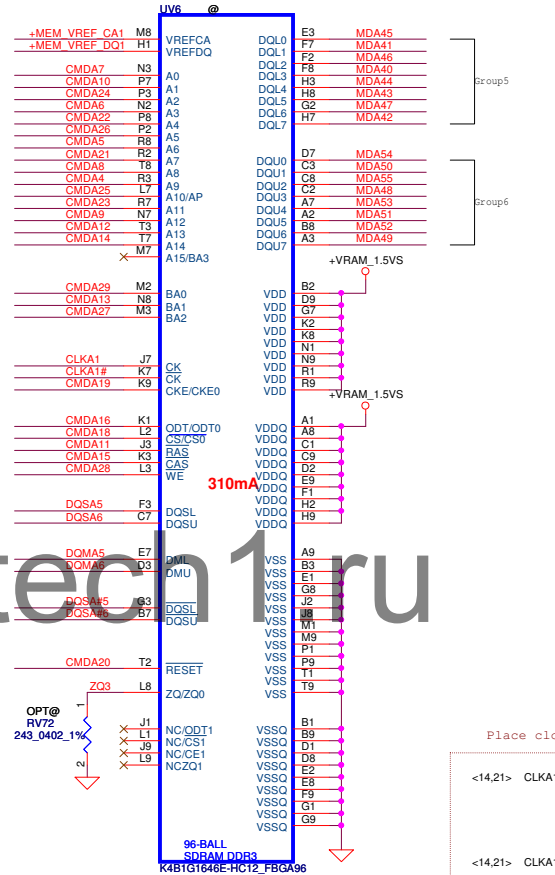
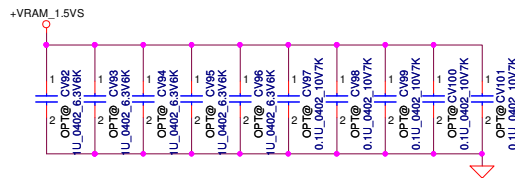
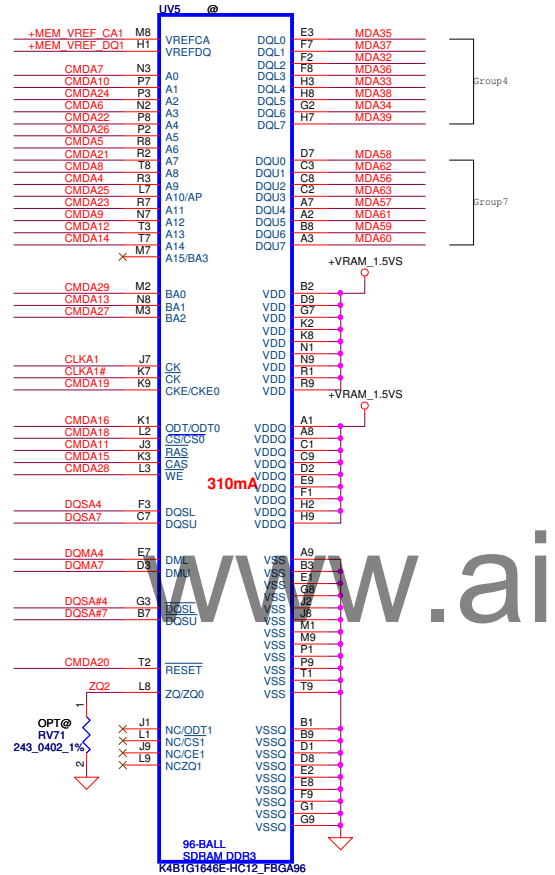
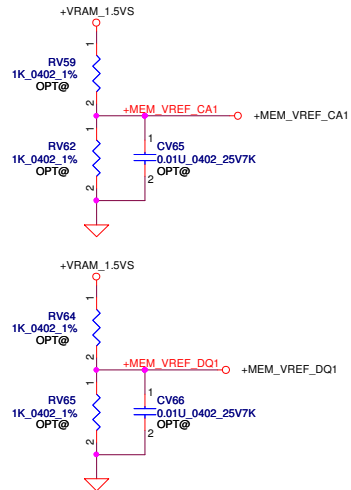


Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

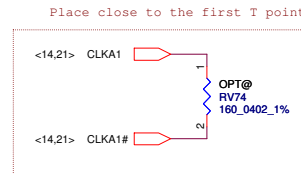


# RANK 0 [63...32] VRAM DDR3 Chips

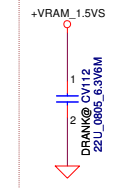
<14,21> DQSA[7..4]  DQSA[7..4]  
<14,21> DQSA#[7..4]  DQSA#[7..4]  
<14,21> DQMA[7..4]  DQMA[7..4]  
<14,21> MDA[63..32]  MDA[63..32]  
<14,18,20,21> CMDA[30..0]  CMDA[30..0]



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE	CKE	
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

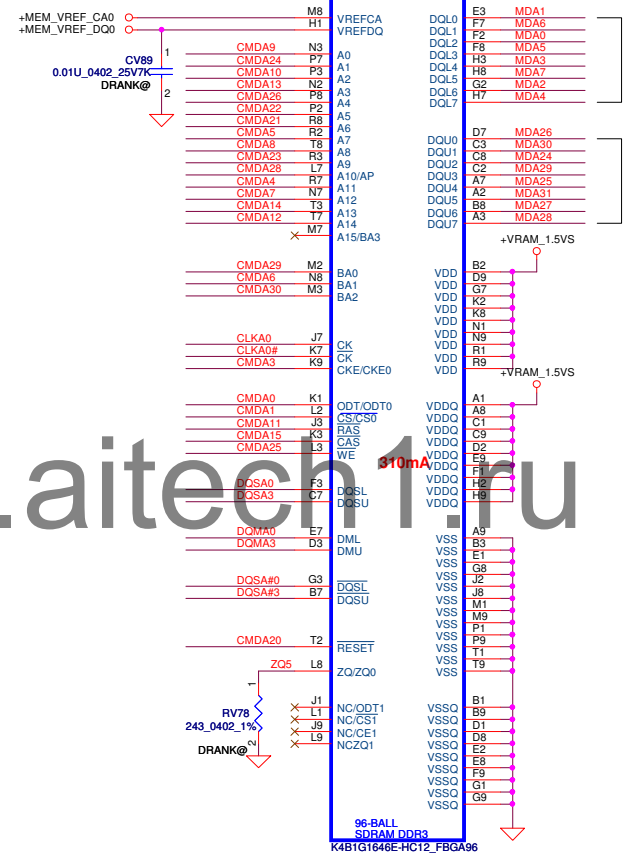
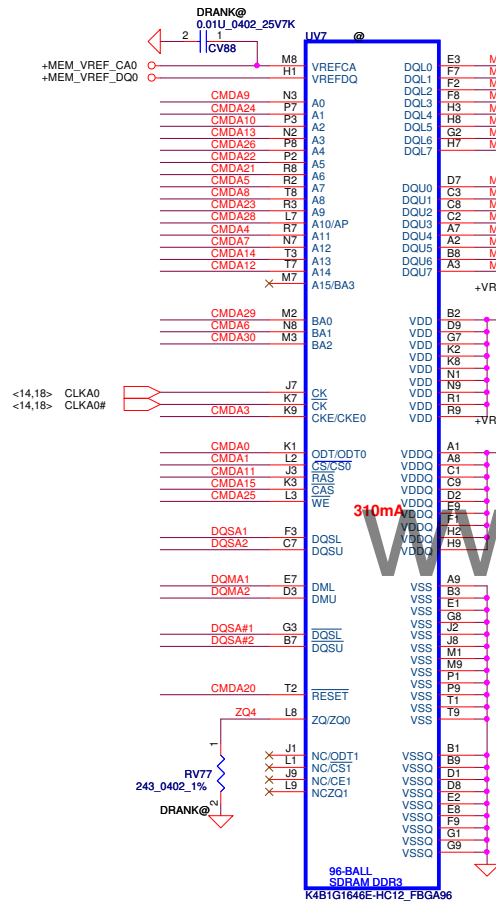
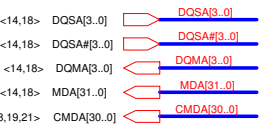


Place close to RANK1 VRAM





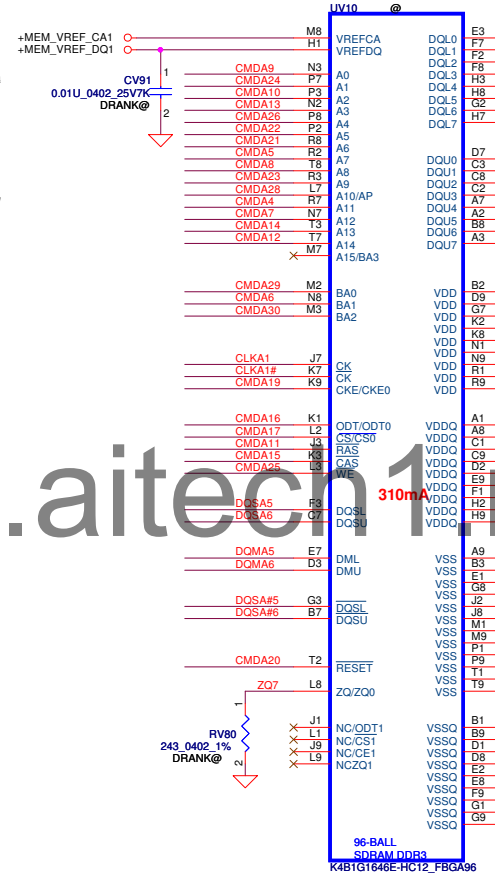
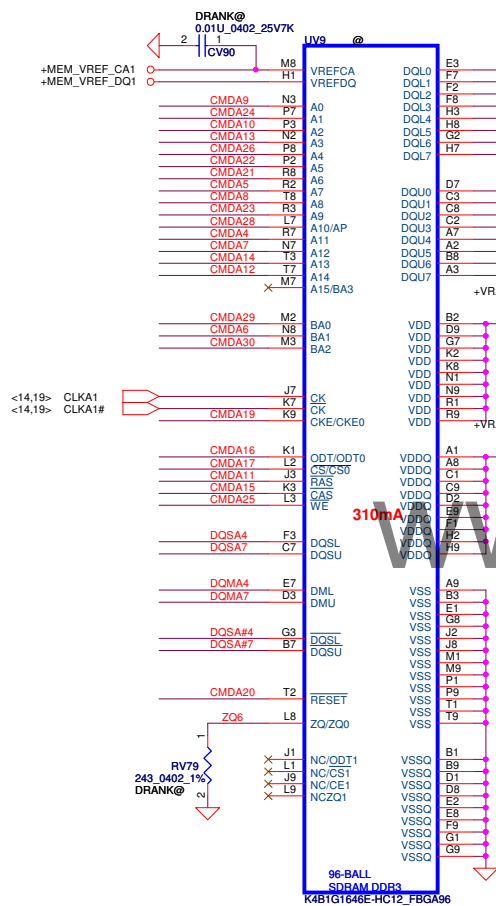
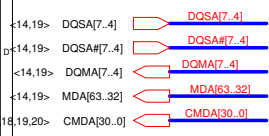
RANK 1 [31...0]  
VRAM DDR3 Chips



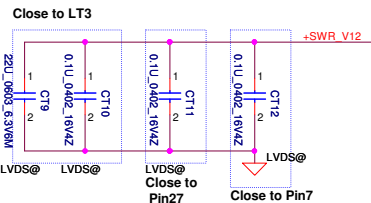
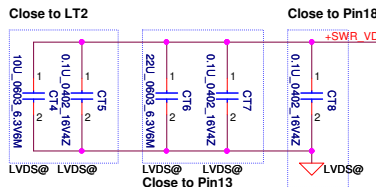
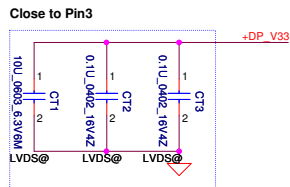
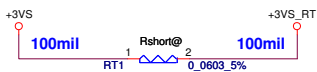
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



RANK 1 [63...32]  
VRAM DDR3 Chips



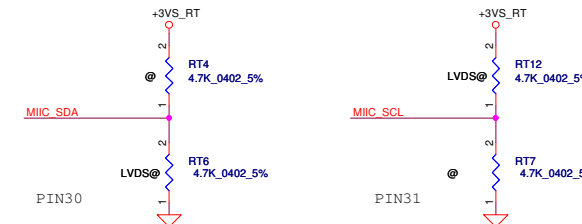
Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17			CS1#	
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2



## Mode Configure

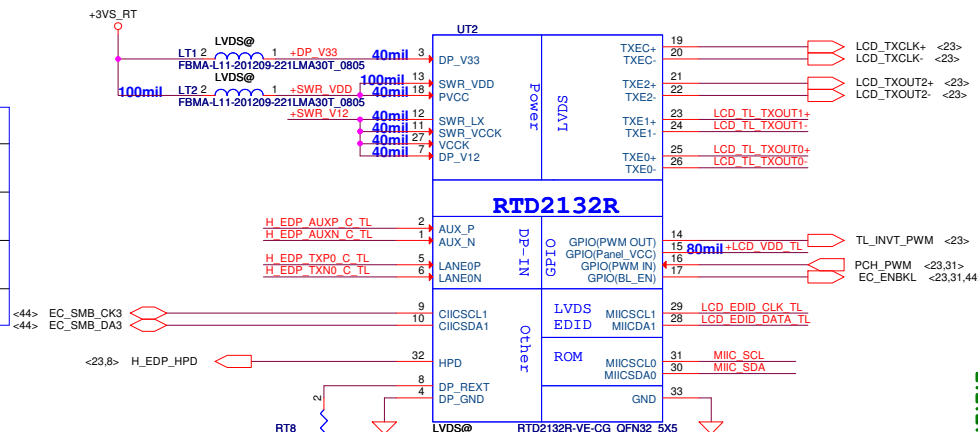
ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.  
 \*\*EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.  
 EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< \*\*Default mode >



SWR / LDO Mode select		
	LDO	SWR
2132S	Do not support	mount LT3
2132R	Use 0 ohm	mount LT3

\* If use 2132R, please select LDO mode as default.



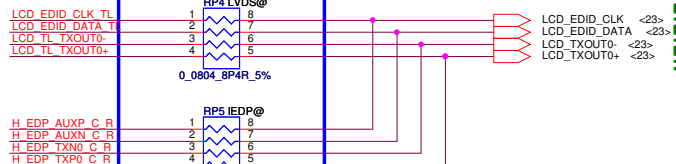
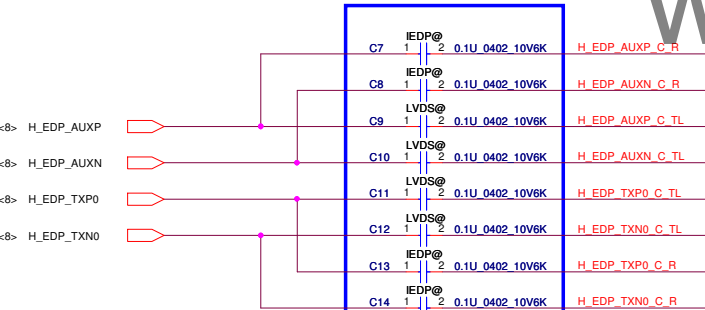
Mode Configure	
ROM only mode	PIN 30 4.7k pull low, Pin 31 4.7k pull high.
**EP mode	PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM	PIN 30 4.7k pull high, Pin 31 4.7k pull high.

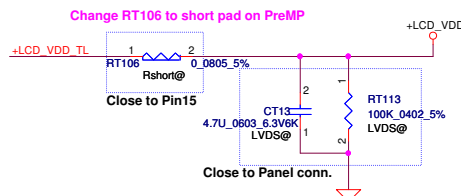
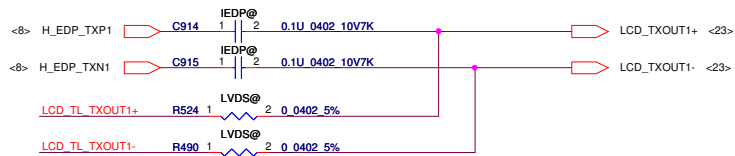
Mode Configure	
ROM only mode	PIN 30 4.7k pull low, Pin 31 4.7k pull high.
**EP mode	PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM	PIN 30 4.7k pull high, Pin 31 4.7k pull high.

Mode Configure	
ROM only mode	PIN 30 4.7k pull low, Pin 31 4.7k pull high.
**EP mode	PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM	PIN 30 4.7k pull high, Pin 31 4.7k pull high.



Place co-layer Resistor back to back on TOP and BOT

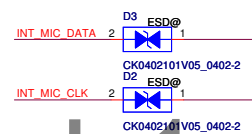
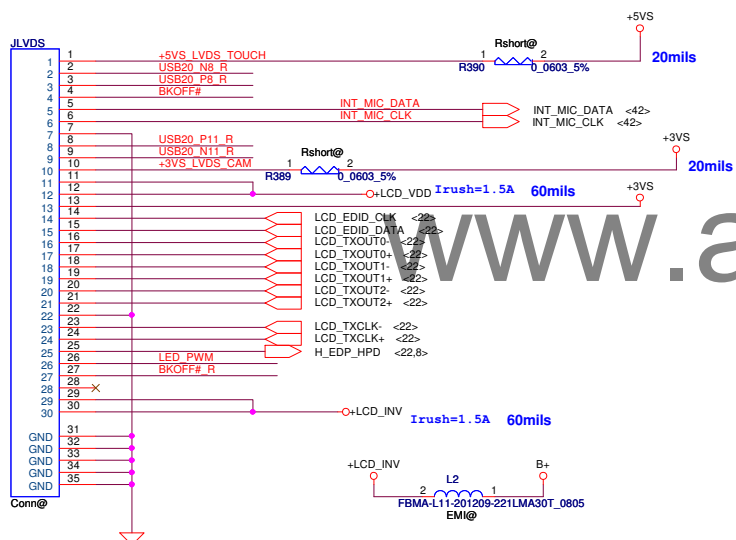


Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

The schematic diagram illustrates the USB20 module's internal components and connections. It features two EMI filters, L57 and L55, each consisting of a common-mode choke and a series resistor (R104 and R105, respectively). The filters are connected to the USB20\_P8\_R, USB20\_N8\_R, USB20\_P11\_R, and USB20\_N11\_R lines. The module also includes an ESD protection diode, D89 (YSLC05CH\_SOT23-3), which is connected to the USB20\_P11\_R and USB20\_N11\_R lines. The diagram shows the module's internal components and their connections to the external USB lines.

When you use 2132R series type of LVDS translator,  
You can delete this portion. If you use 2132S, please don't.

The schematic diagram shows the LCD driver circuit for the APL3512AB1-TRG\_SOT23-5. The circuit includes a +3VS supply, a +LCD\_VDD supply, and a +LCD\_VDD\_SS supply. The APL3512AB1-TRG\_SOT23-5 IC is connected with VIN to +LCD\_VDD, SS to +LCD\_VDD\_SS, and EN to a control signal. The output VOUT is connected to the LCD panel through a resistor R83 (0.3805\_5%) and a short circuit Rshort. The LCD panel is also connected to a resistor R112 (100K\_0402\_5%) and a control signal LCD\_ENVDD <31>.



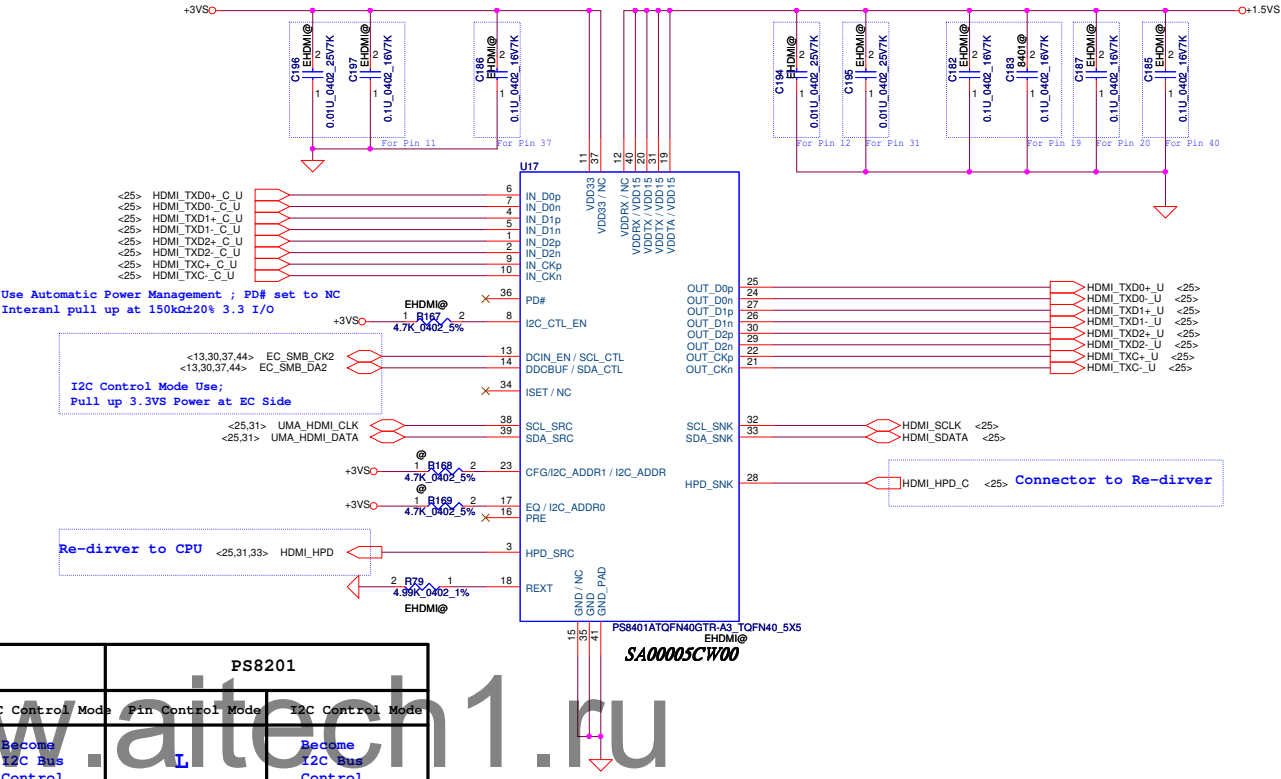
Reserve for LVDS panel

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				Custom	1.0	
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Default to PS8401 & PS8201 I2C Control Mode

I2C Mode HDMI ID Setting

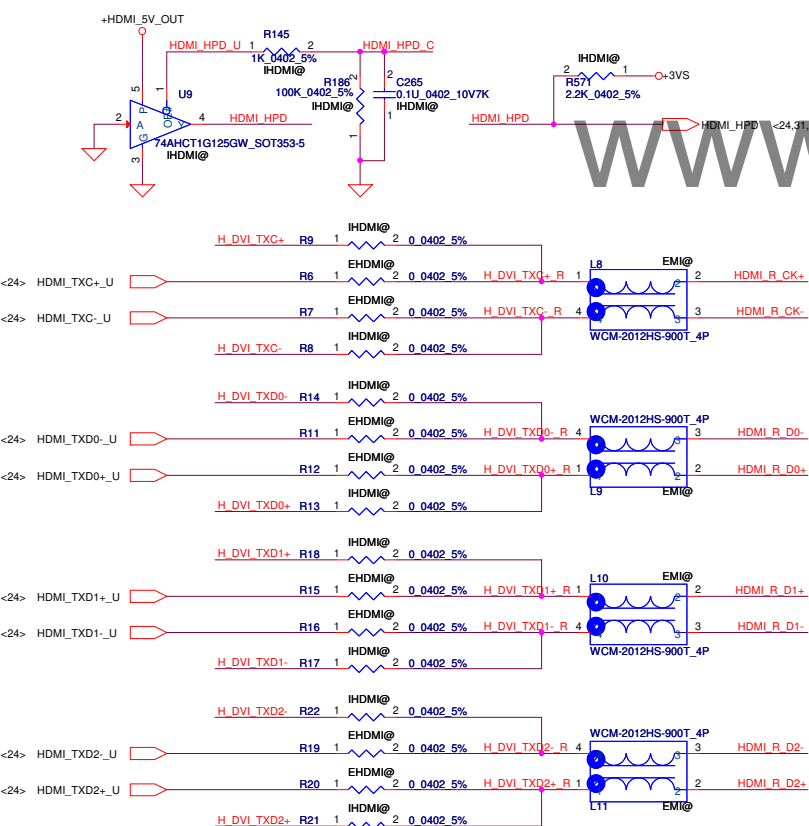
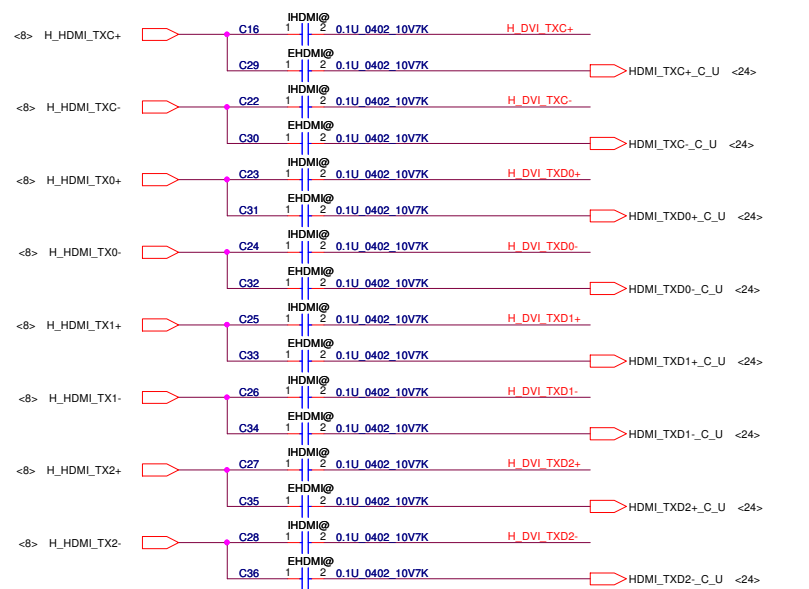
If PS8401 use I2C Mode , EQ=I2C\_ADDR0 , CFG = I2C\_ADDR1  
For PS8401  
I2C control bus address LSB; Internal pull down at 150kohz±20%, 3.3V I/O.  
[I2C\_ADDR1, I2C\_ADDR0] ; I2C Address (W/R)=  
LL: 0x4C/4D (default)  
LH: 0x5C/5D  
HL: 0xCC/CD  
HH: 0xEC/ED  
  
If PS8401 use I2C Mode , EQ=I2C\_ADDR  
For PS8201  
I2C control bus address LSB; Internal pull down at ~150k ohz, 3.3V I/O.  
[I2C\_ADDR] ; I2C Address (W/R)=  
L: 0x64/65 (default)  
H: 0xE4/E5



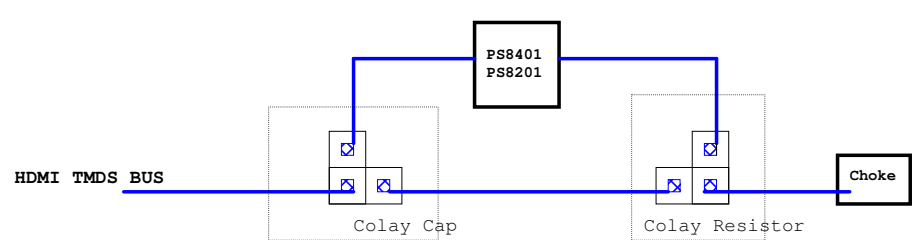
Strap H:3.3V M:1.65V L:0V

Net name	Description	PS8401		PS8201	
		Pin Control Mode	I2C Control Mode	Pin Control Mode	I2C Control Mode
DCIN_EN	DC coupling enable; Internal pull down at 150k ohz ±20%, 3.3V I/O. L: default, AC coupling input H: DC coupling input	L	Become I2C Bus Control	L	Become I2C Bus Control
DDCBUF	Enable active DDC buffer; Internal pull down at 150k±20%, 3.3V I/O. L: default, passive DDC pass-through H: active DDC buffer with default threshold M: active DDC buffer without internal pull up resistor	M	Become I2C Bus Control	M	Become I2C Bus Control
ISET	TMDS output swing adjustment; Internal pull down at 150k±20%, 3.3V I/O. For PS8401 Only ISET = L: Default H: Increase +13% M: Reduce -13%	L	NC	NC	NC
CFG	CFG: Configuration pin, 3.3V IO, internal pull down at 150k±20%. 3.3V I/O CFG = L: HDMI ID disable H: HDMI ID enable	H	NC	H	NC
EQ	EQ:Receiver equalization setting;; Internal pull down at ~150k?, 3.3V I/O For PS801 EQ = L:programmable EQ for channel loss up to 6.5dB @ 3.0Gbps H:programmable EQ for channel loss up to 9.5dB @ 3.0Gbps M:programmable EQ for channel loss up to 3dB @ 3.0Gbps  For PS8401 EQ = L:programmable EQ for channel loss up to 12.4dB H:programmable EQ for channel loss up to 4.3dB M:programmable EQ for channel loss up to 0.6dB	M	NC	M	NC
PRE	Output pre-emphasis setting; Internal pull down at 150k±20%, 3.3V I/O. PRE = L: No pre-emphasis H: 1.6dB pre-emphasis M: 2.5dB pre-emphasis	L	NC	L	NC
I2C_CTL_EN	I2C Control enable. Internal pull down at 150k±20%. 3.3V I/O I2C_CTL_EN = LOW (L): Pin Control is selected. HIGH (H): I2C Control is selected.	L	H	L	H

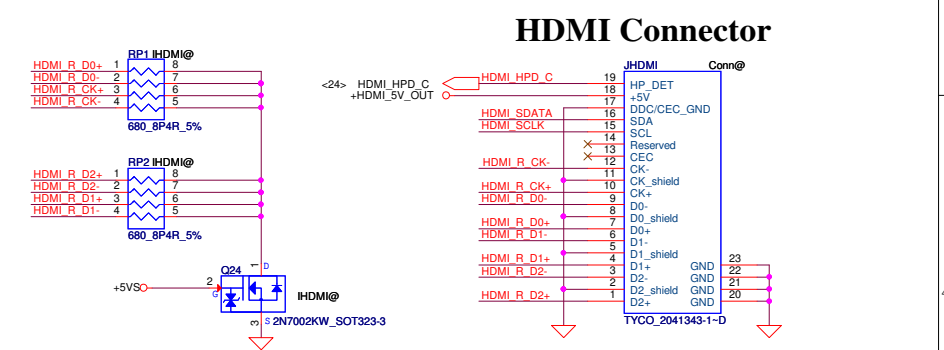
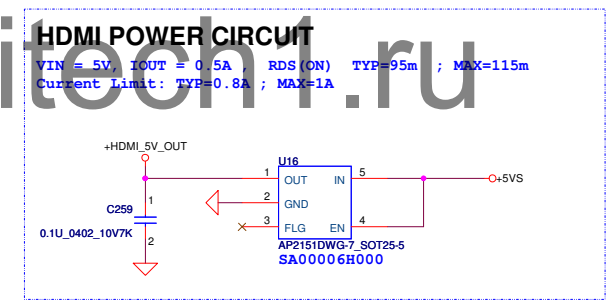
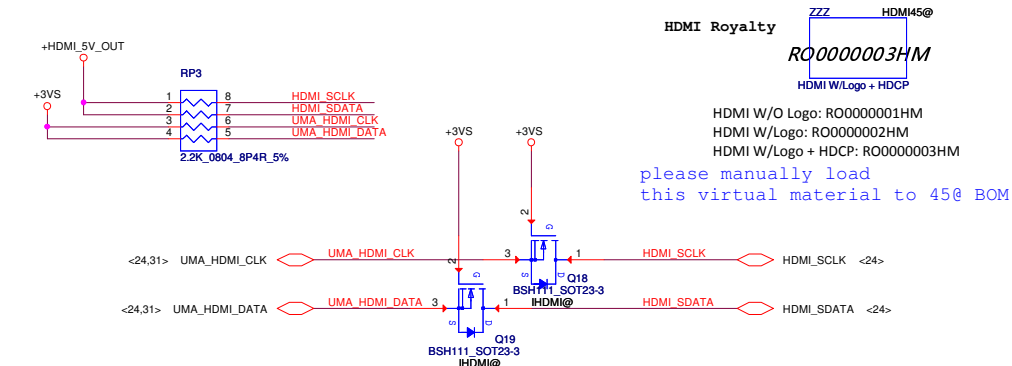
Note: PS8401 have Jitter cleaning function and can control TMDS output swing , PS8201 don't have.



Common CHOKE use 90ohm

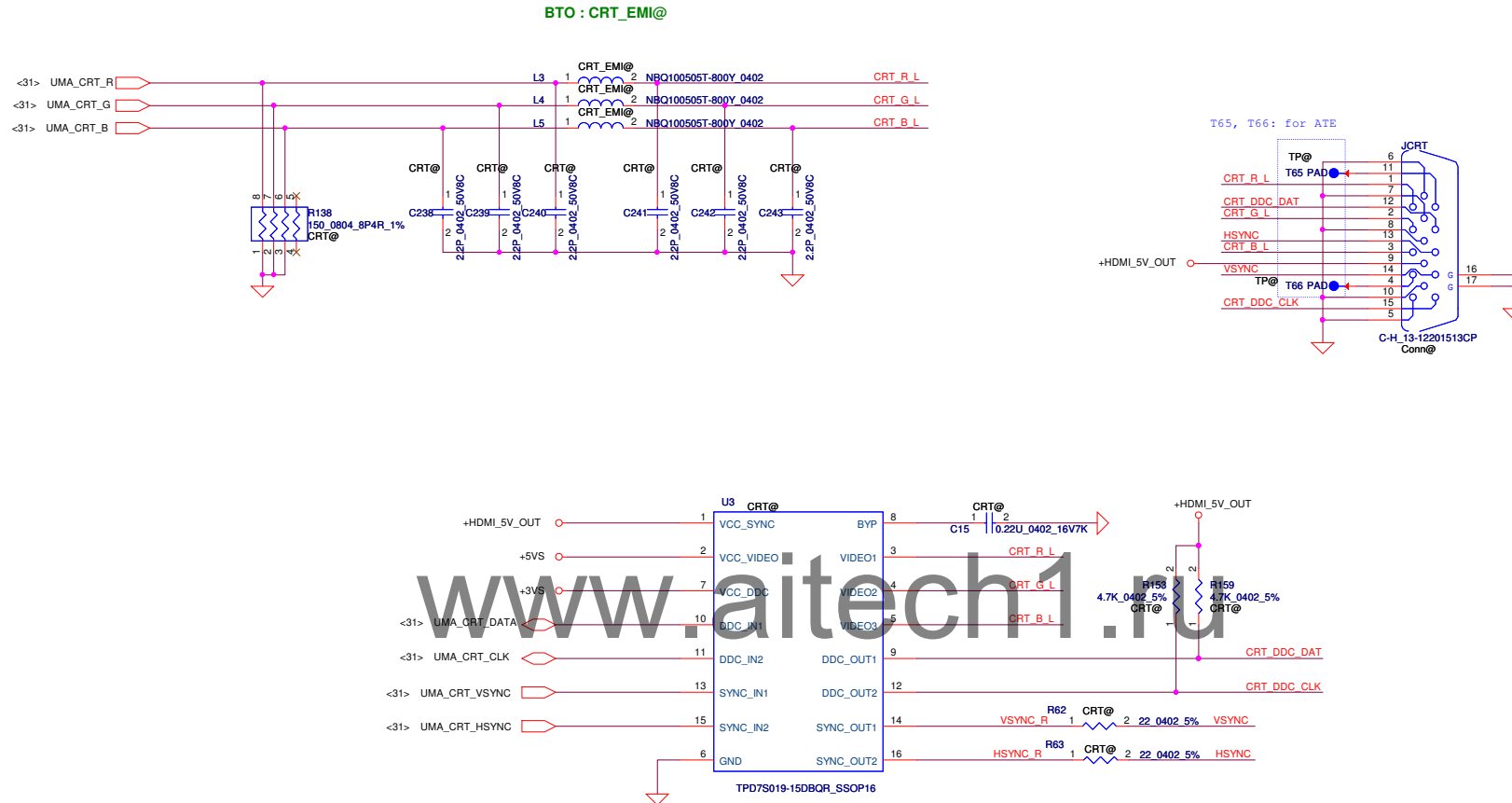


Componet close to Conn.  
Impedance depend on platform design guide

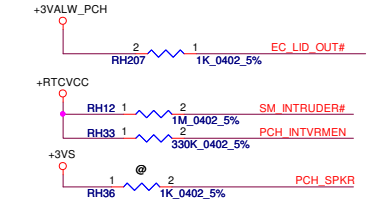
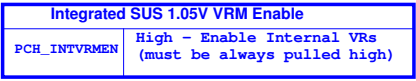
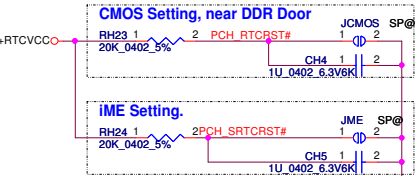


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								2015/04/19			
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## ***CRT CONNECTOR***



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				VSKAA	
Date: Thursday, May 09, 2013		Sheet 26 of 57			



**PCH\_SPKR**

High = Enabled "No Reboot Mode"

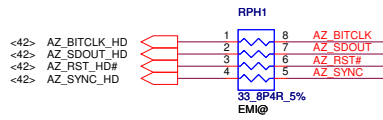
Low = Disabled (Default)

**HDA\_SDO**

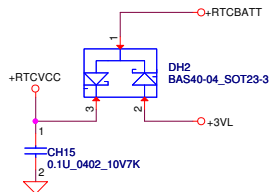
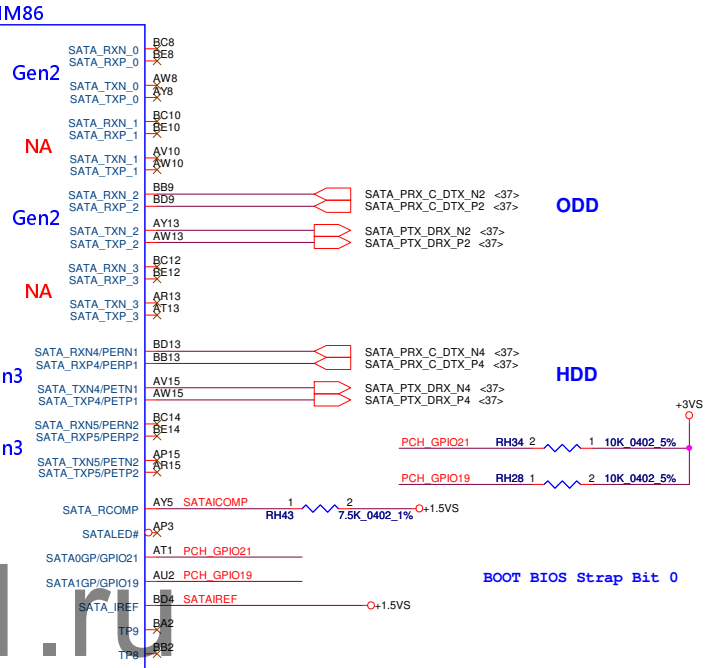
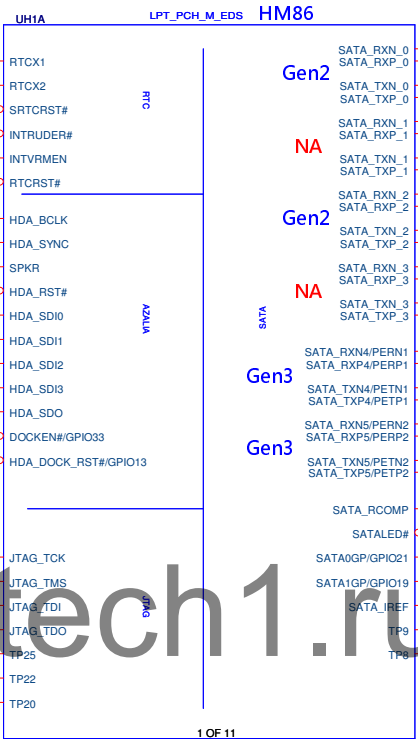
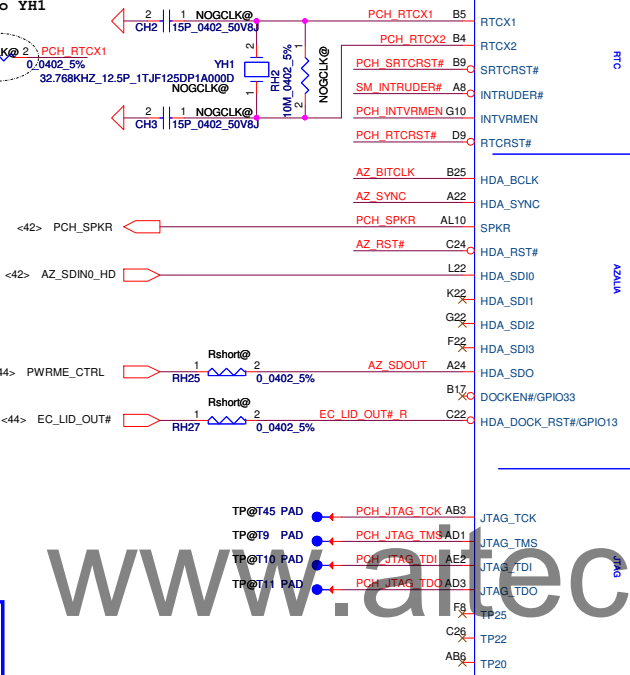
ME debug mode, this signal has a weak internal pull down

★Low = Disable (default)

High = Enable (flash descriptor security override)



Placement near to YH1

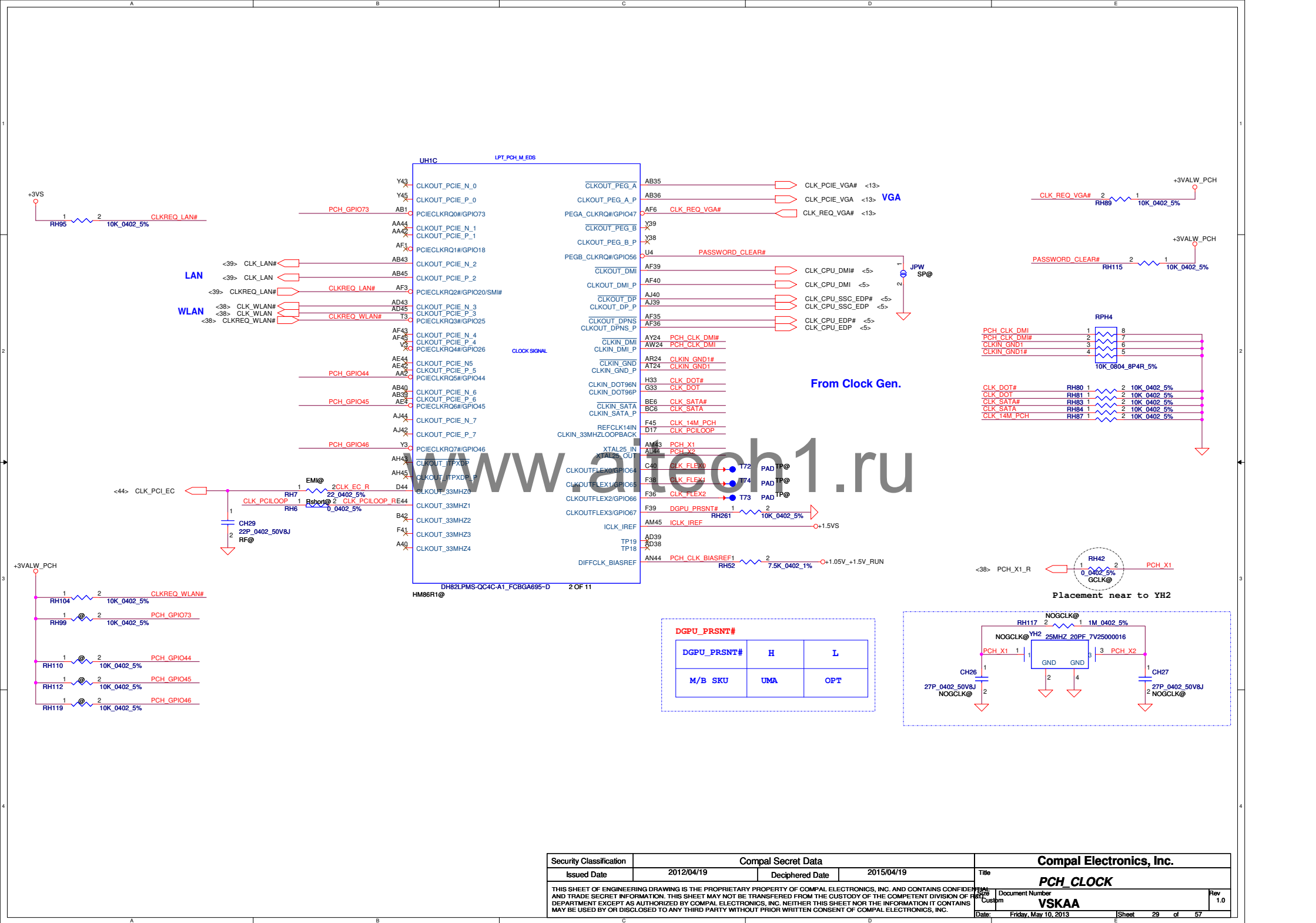


Un-mount for reduce power consumption at S0, S3 state

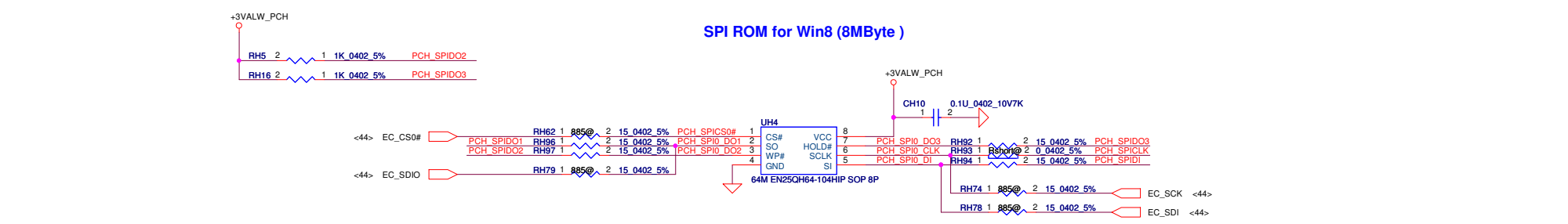
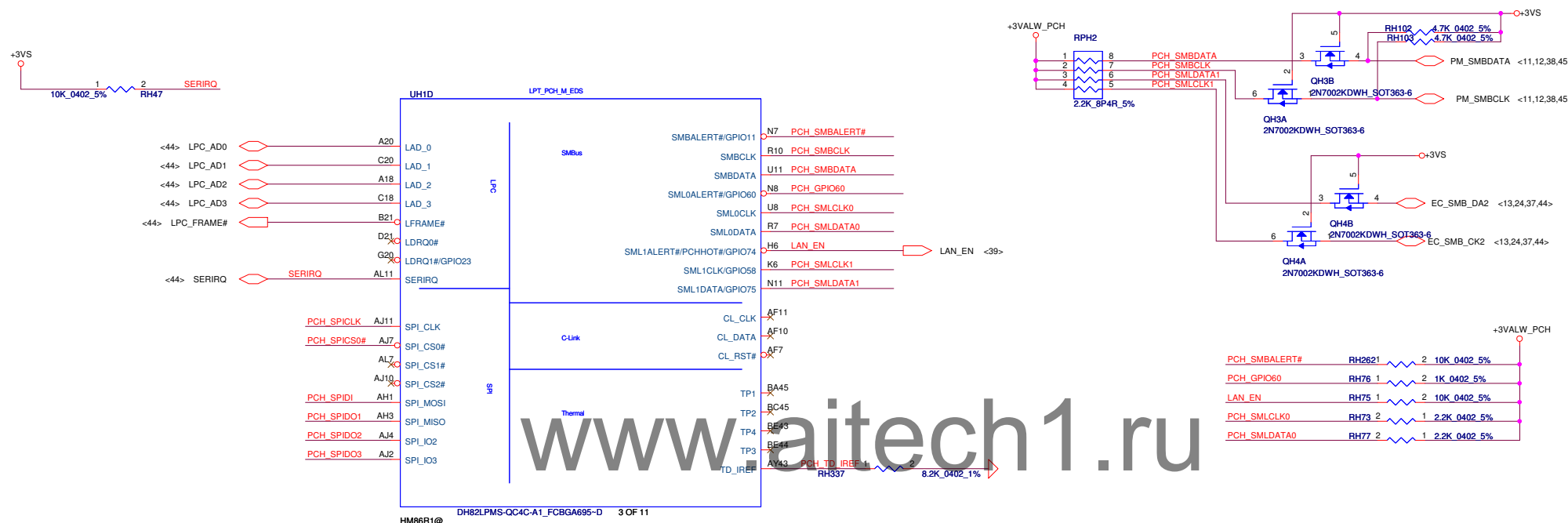
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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	PCH_HDA/JTAG/SATA		
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				Custom	VSKAA		
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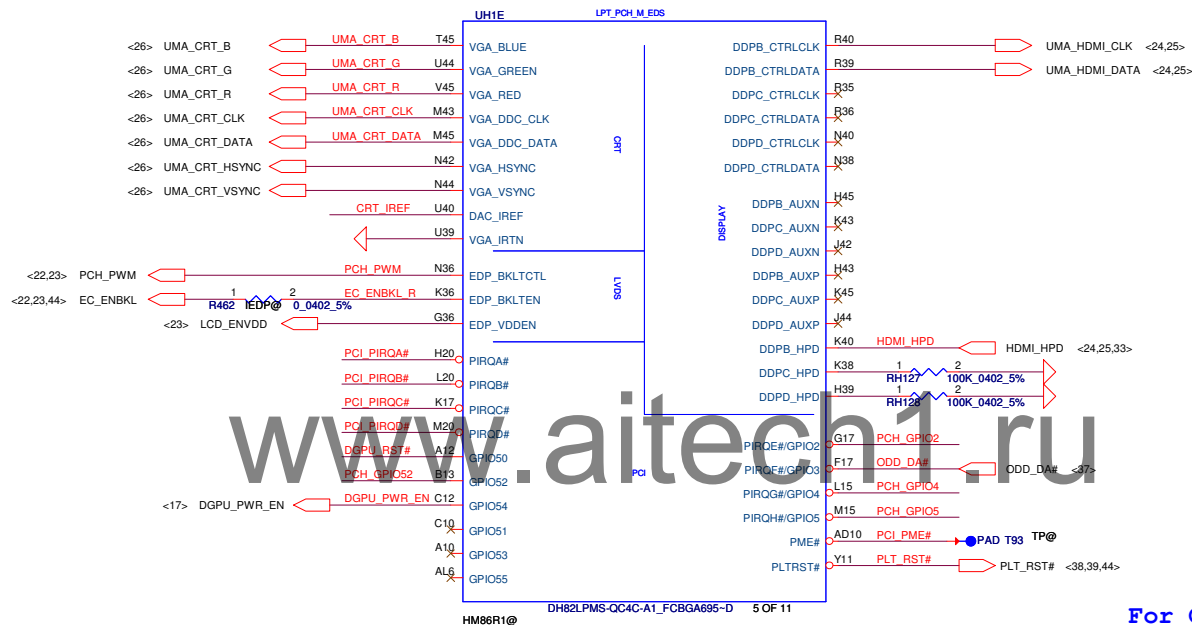
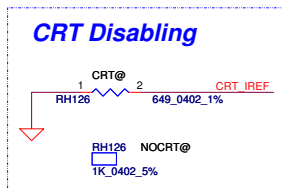
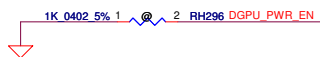
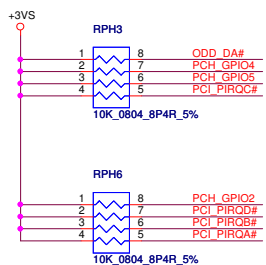
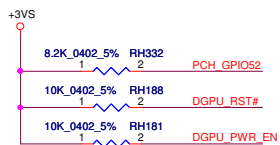
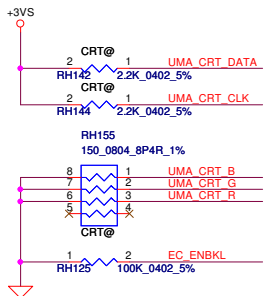


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	<b>PCH_CLOCK</b>
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				Custom	1.0
Date:				Friday, May 10, 2013	Sheet 29 of 57



Socket: SP07000F500/SP07000H900  
Please place UH4 close to UH1 PCH

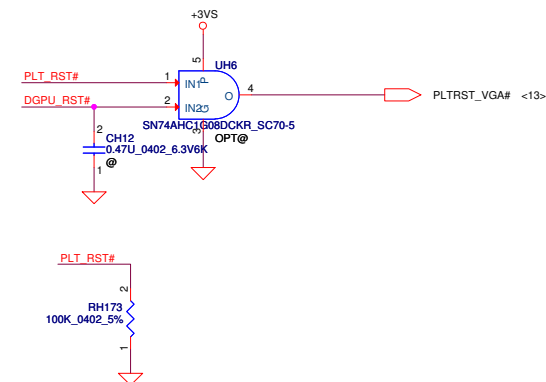
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2012/04/19		Deciphered Date		2015/04/19		Title		PCH LPC/SPI/SMBUS			
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								Custom		VSKAA		1.0	
								Date		Friday, May 10, 2013		Sheet	
C				D				E		30		of 57	



Boot BIOS Strap		
RF_OFF# PCH_GPIO19	PCH_GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI ★

A16 Swap Override Strap	
WL_OFF#	Low= A16 swap override Enable High= A16 swap override Disable
★	

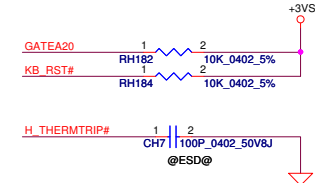
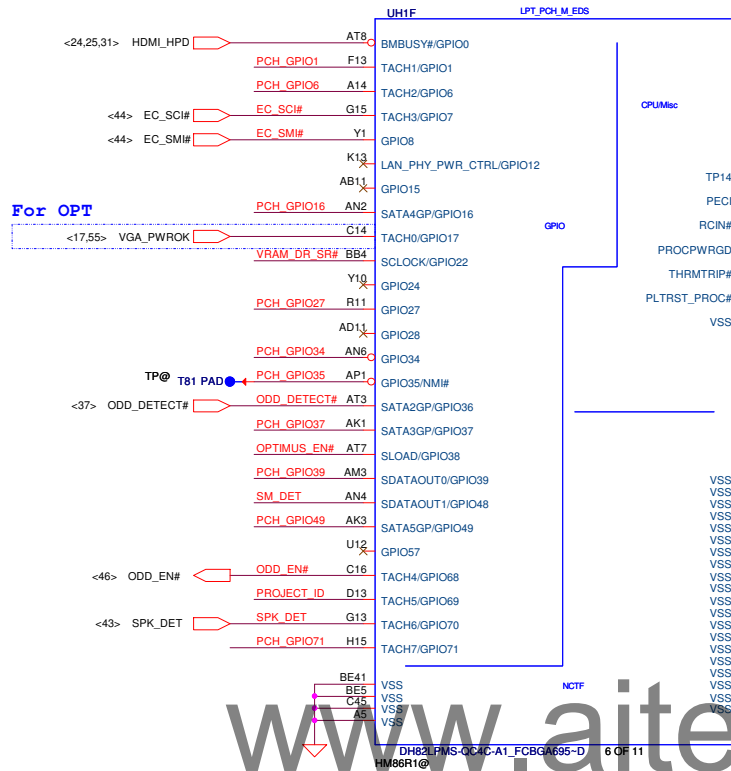
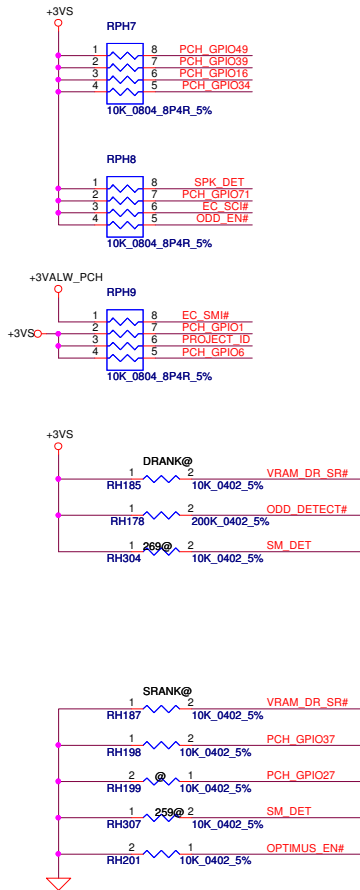
For Optimus



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Issued Date	2012/04/19	Deciphered Date	2015/04/19	Title	PCH_CRT/LVDS/HDMI/PCI
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				Date	Friday, May 10, 2013
				Sheet	31 of 57



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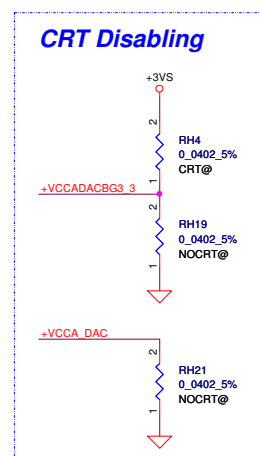
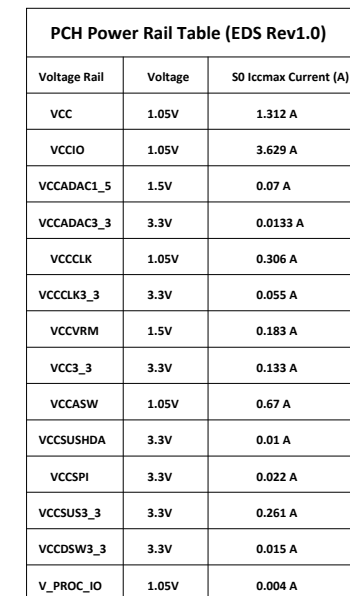
OPTIMUS_EN#		
OPTIMUS_EN#	H	L
SKU	UMA	Optimus

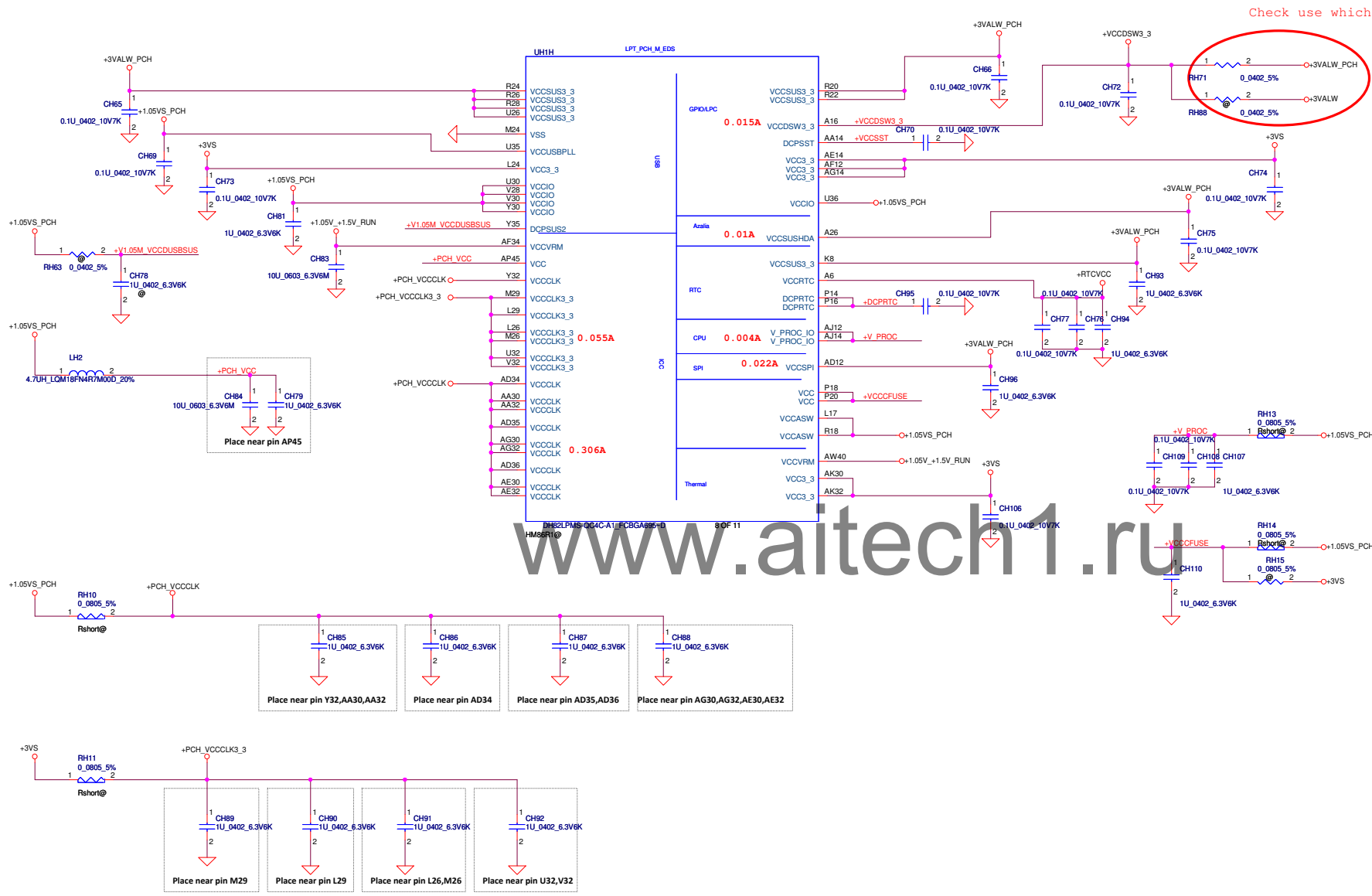
PROJECT_ID		
PROJECT_ID	H	L
SKU	SharkBay SV	SharkBay ULT

SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

Follow Compal ORB  
and Intel Check list 460603 V1.5

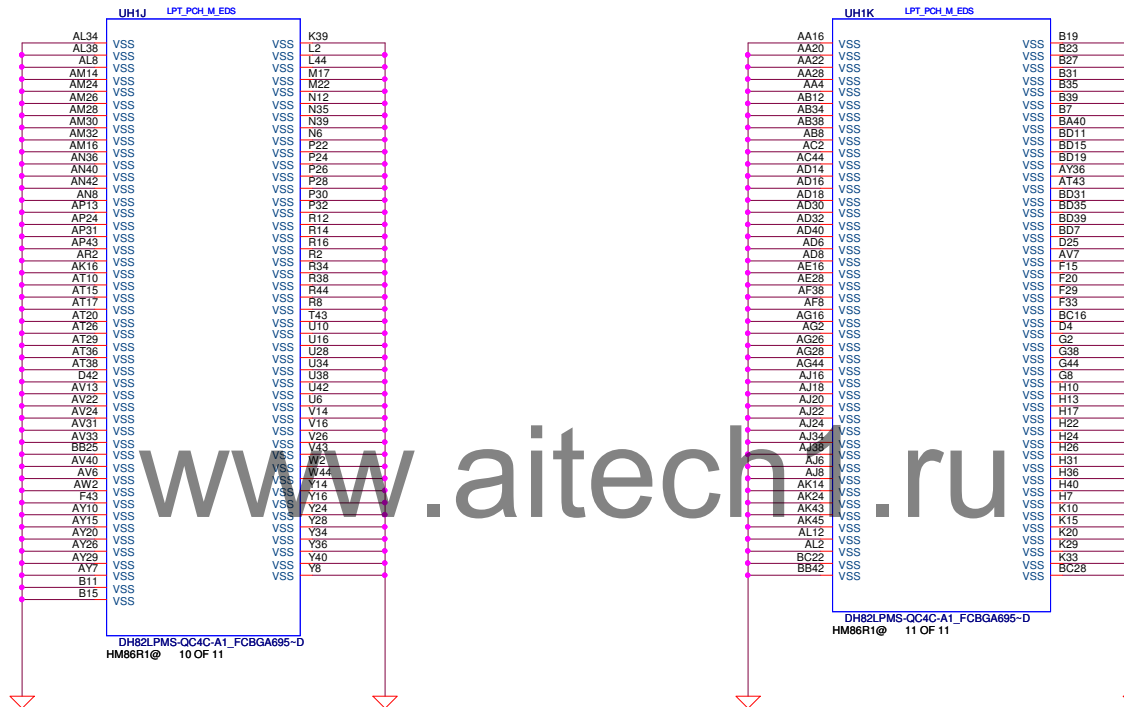




Check use which power rail

PCH Power Rail Table (EDS Rev1.0)

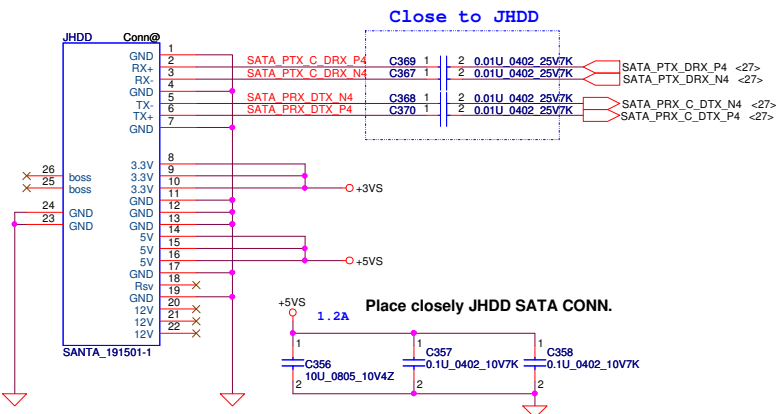
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.07 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



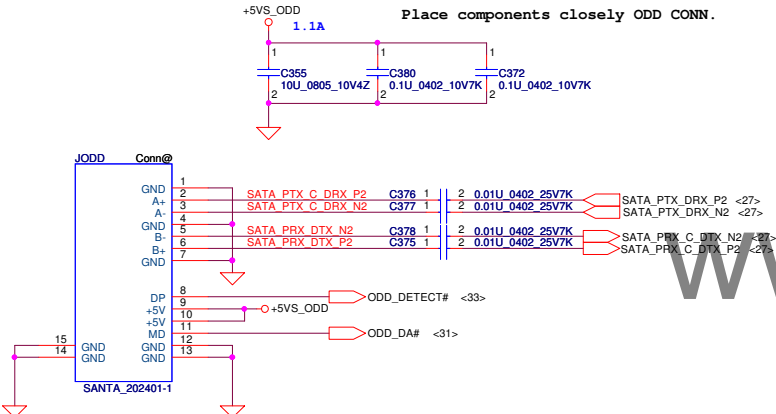
Security Classification				Compal Secret Data		Compal Electronics, Inc.		
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				Date	Friday, May 10, 2013	Sheet	36	of 57



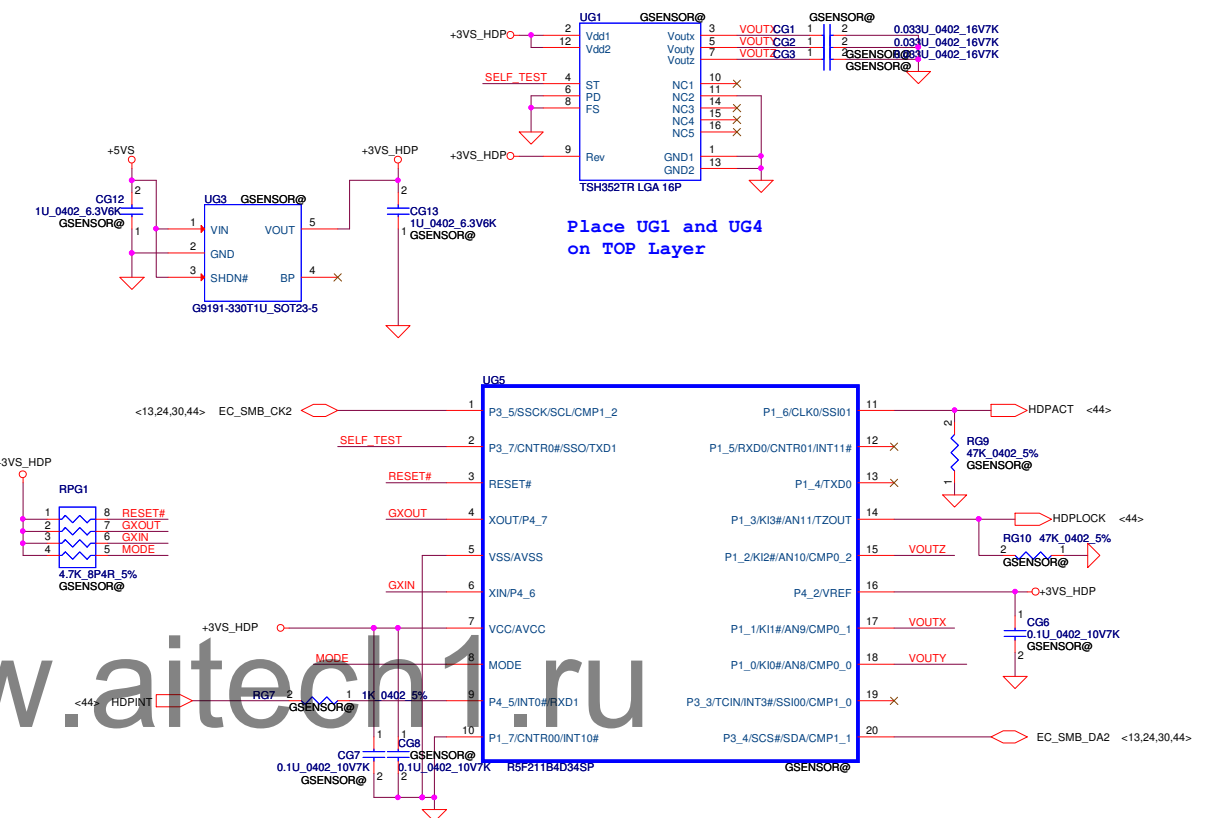
SATA HDD Conn.



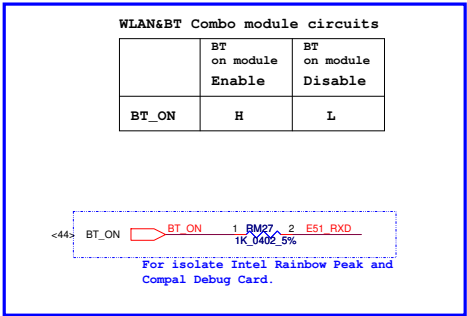
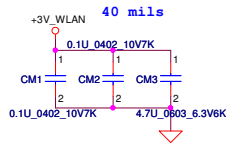
SATA ODD Conn



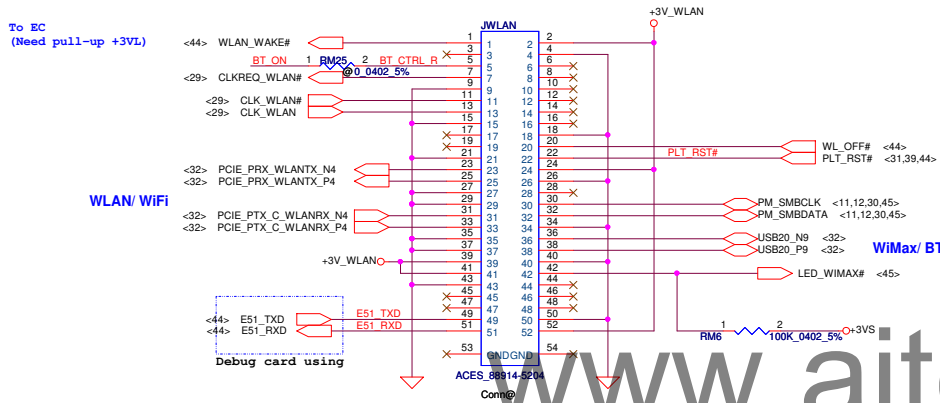
G-Sensor



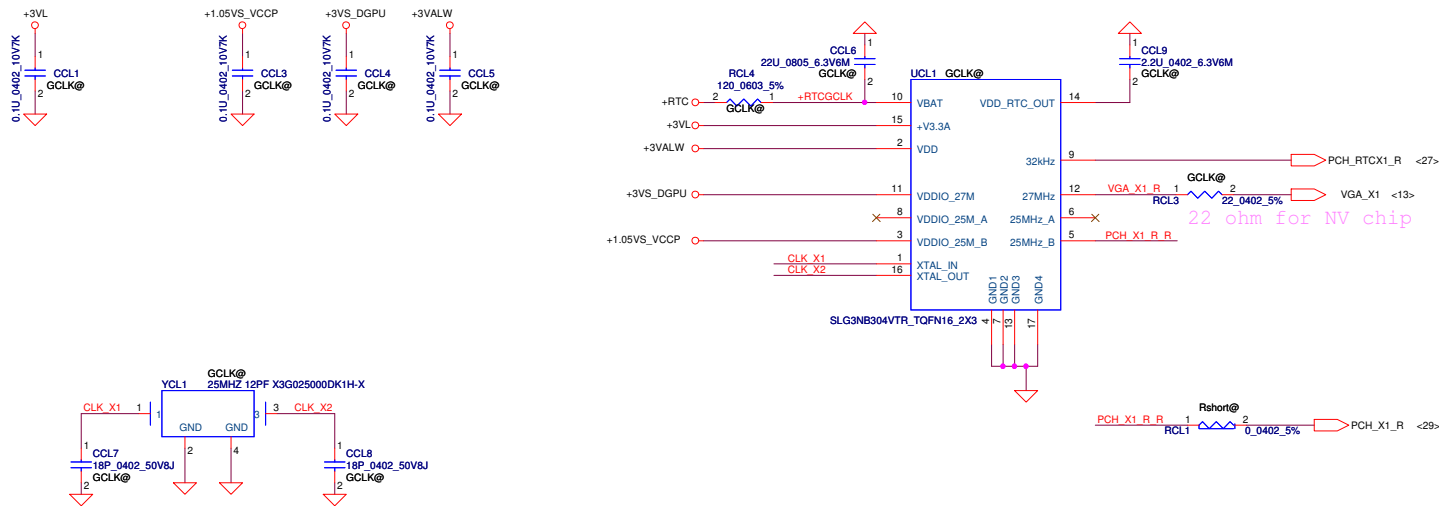
Slot 1 Half PCIe Mini Card-WLAN



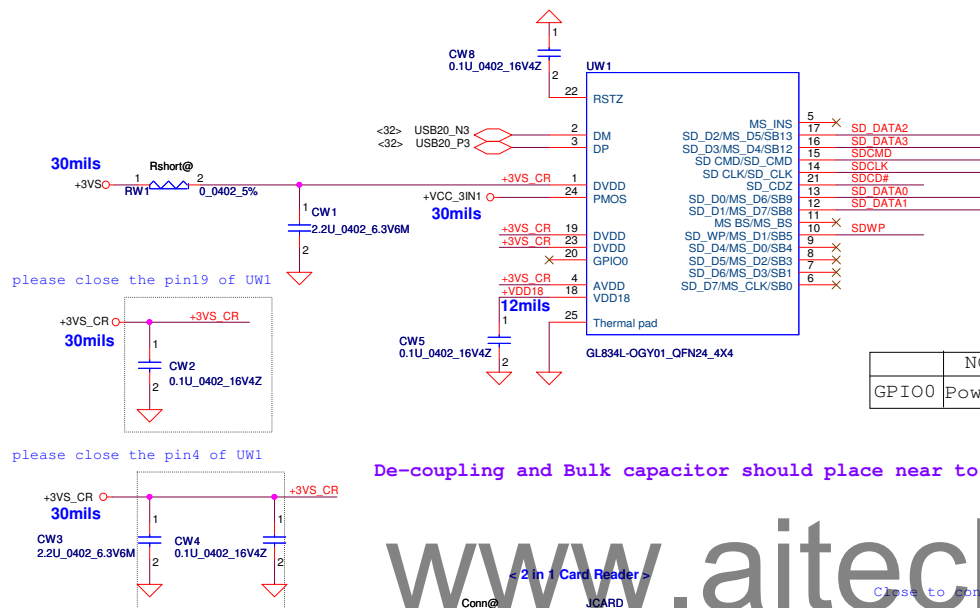
Slot 2 Full PCIe Mini Card- mSATA 14" no support



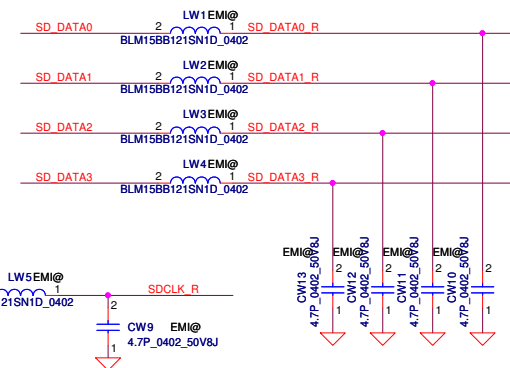
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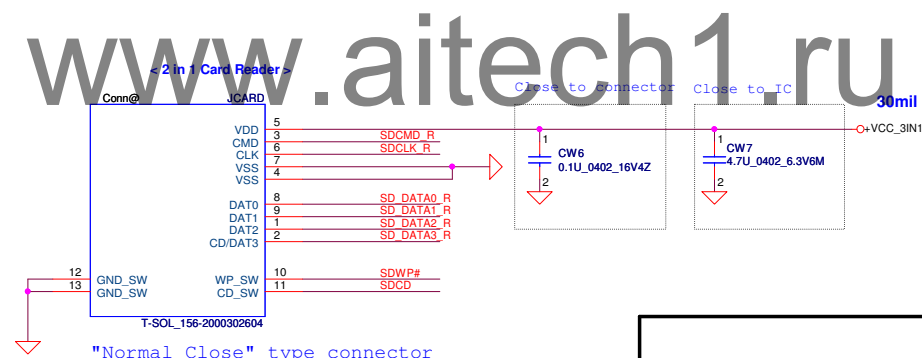


For EMI request  
(Place close to chip)



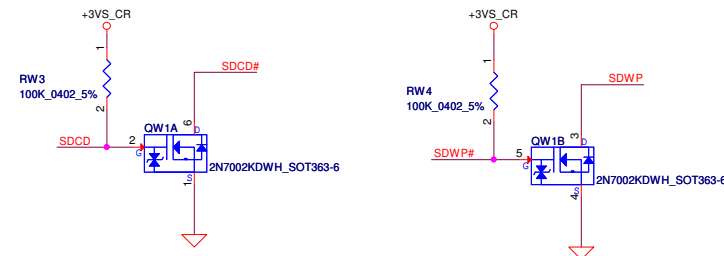
	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

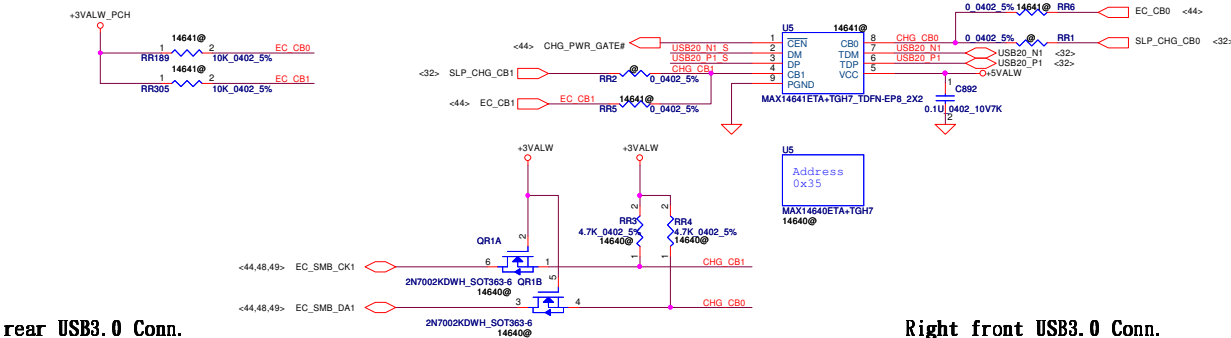
De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



	CD_SW	WP_SW	
Card Uninsertion	Close	Protect disable	Protect Enable
		Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit

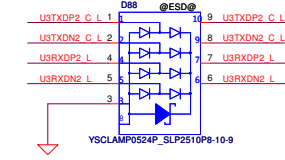
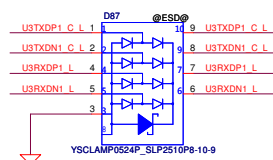
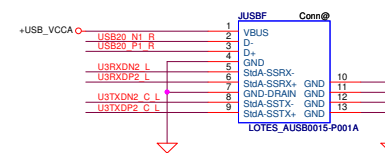
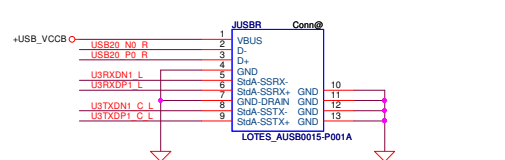
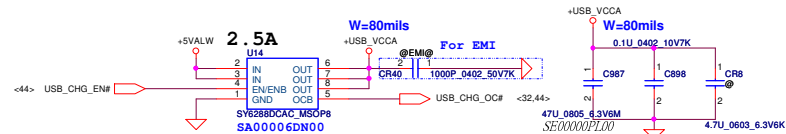
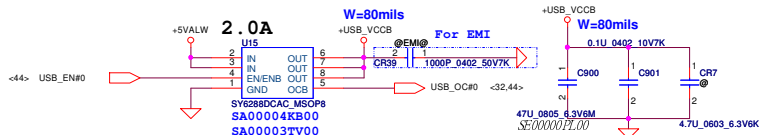
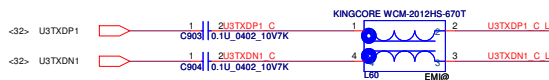
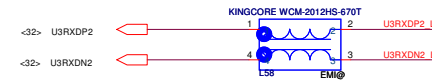
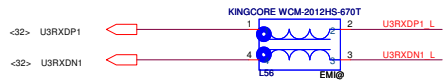
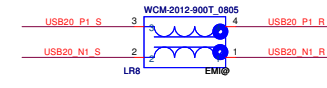
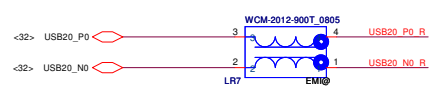


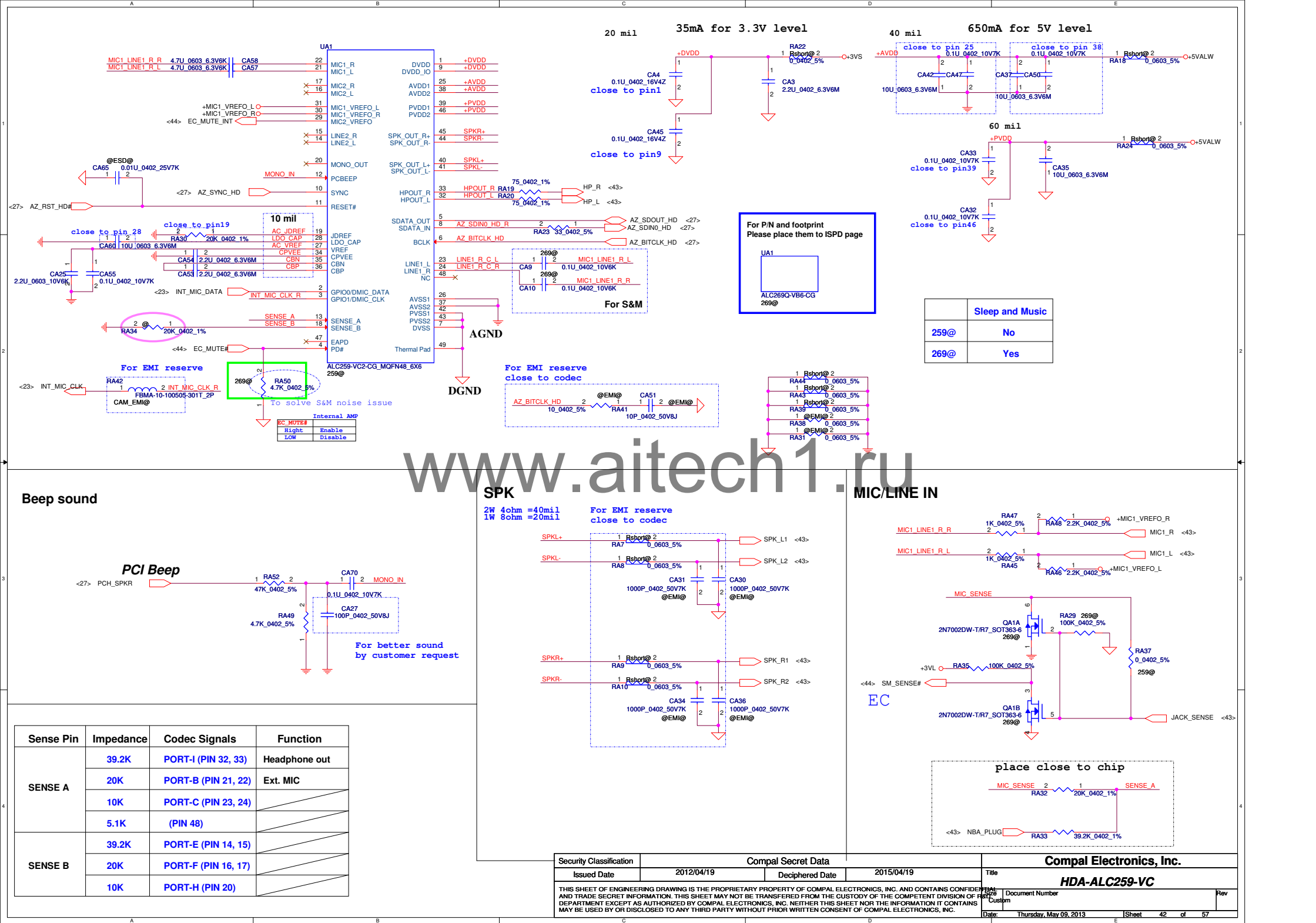


Right rear USB3.0 Conn.

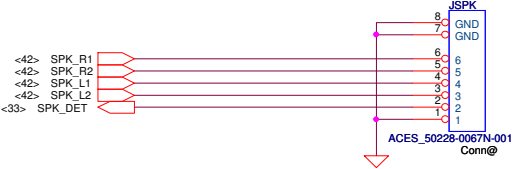
Right front USB3.0 Conn.  
(Support S&C function)

State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.





SPK Conn.

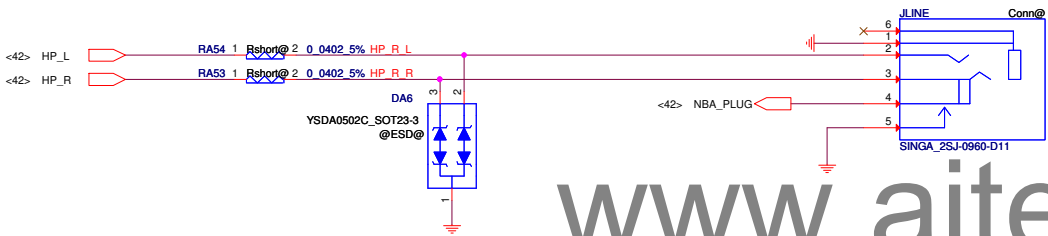


SM_DET	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
		Non Harman	259@



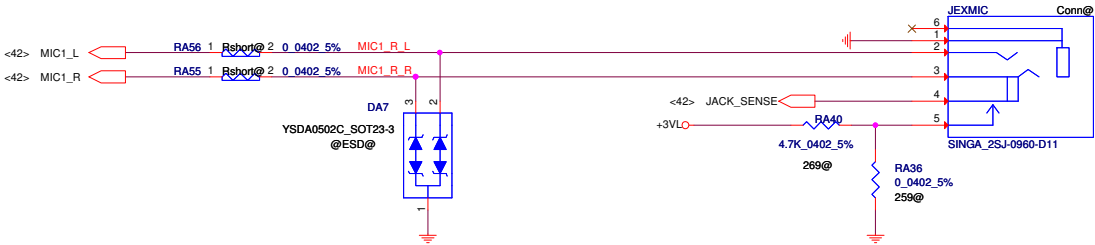
Non-Harman detection		
SPK_DET	0	ONKYO
	1	Non-Brand

HeadPhone/LINE Out JACK

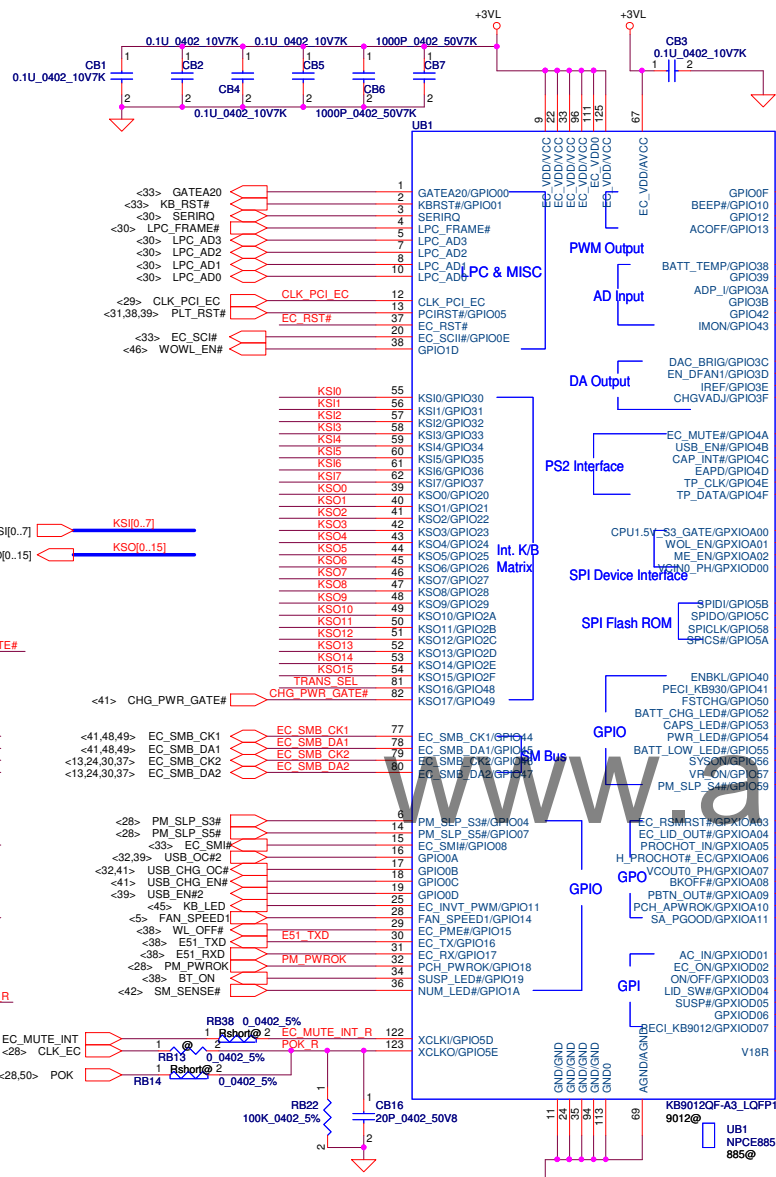
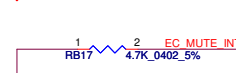
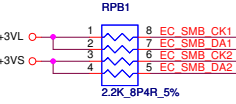
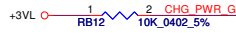
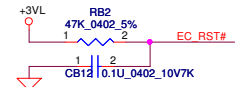
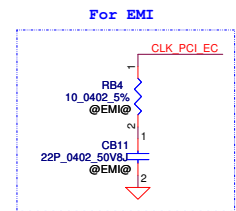


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MIC/LINE IN JACK

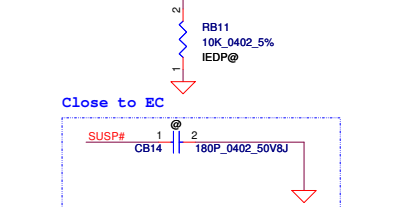
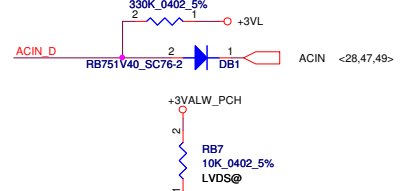
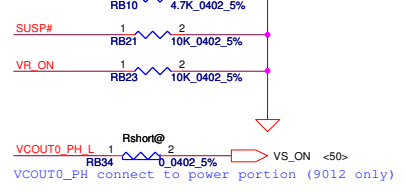
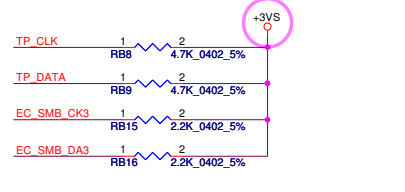
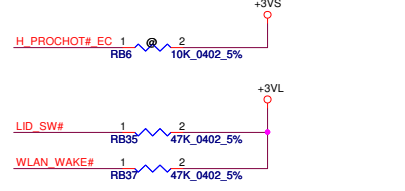
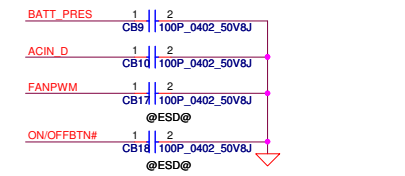
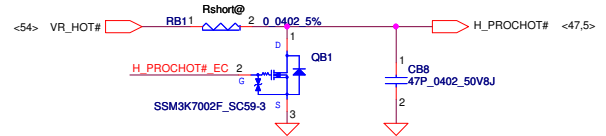
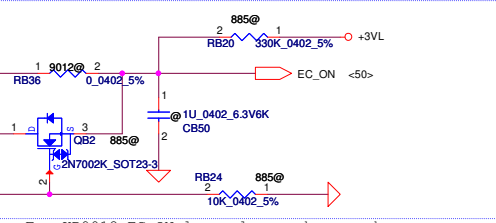


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								Document Number		Rev 1.0	
								Date: Thursday, May 09, 2013		Sheet 43 of 57	



**Voltage Comparator Pins FOR 9012 A3**

VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102	HIGH (default)	LOW
VCOUT0 pin104	HIGH	LOW (default)
VCOUT1 pin103	HIGH	LOW (default)



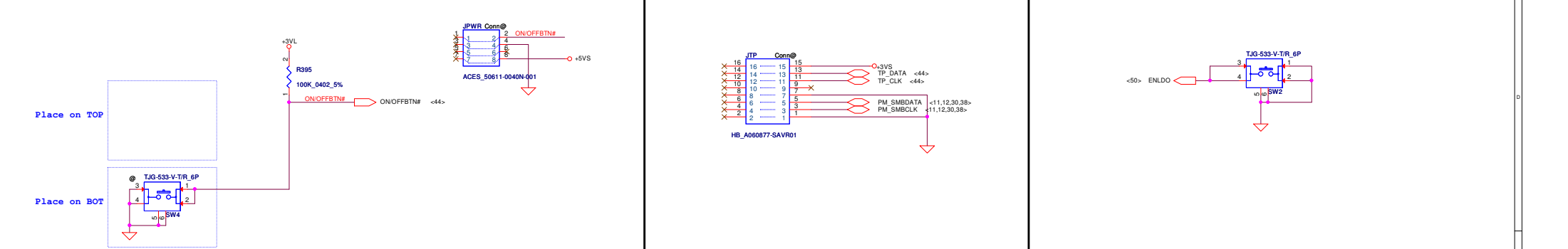


Power Button

Conn.

Touchpad Connector

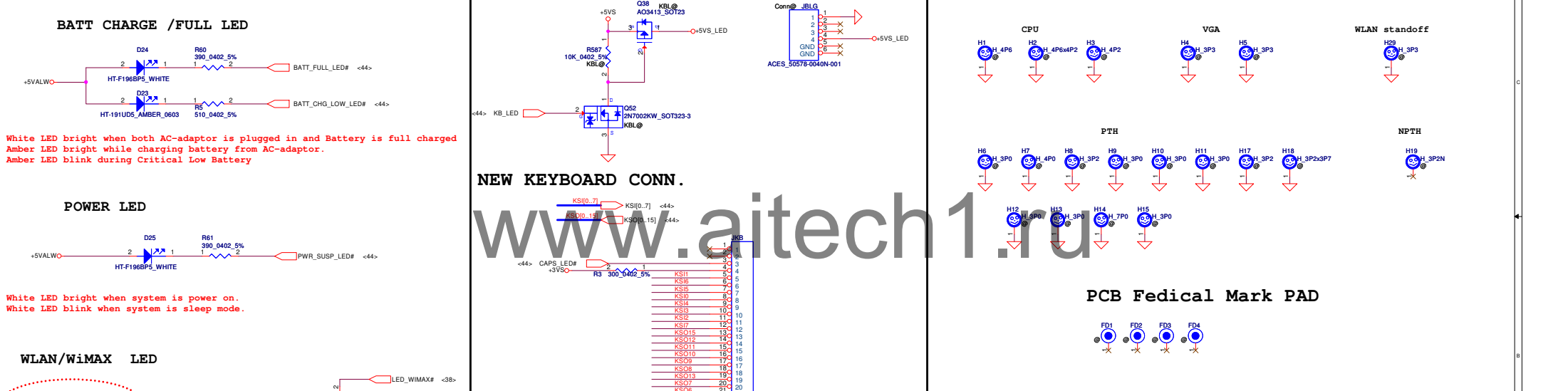
Battery Reset



LED/LID

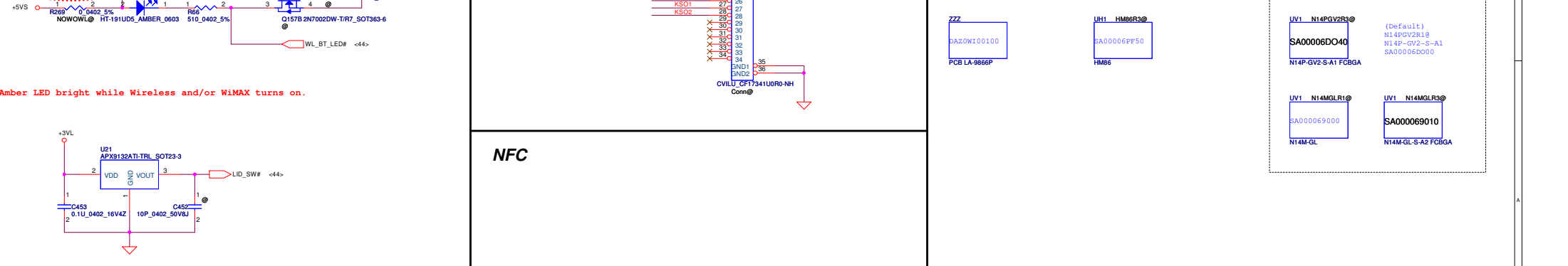
Keyboard LED

Screw Hole

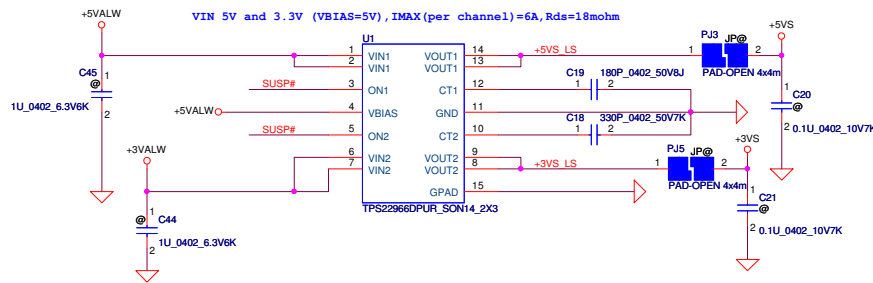


ISPD

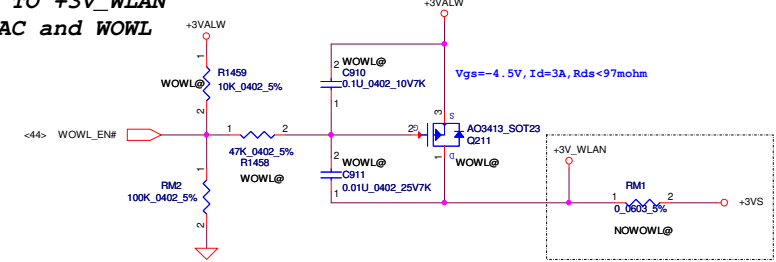
GPU



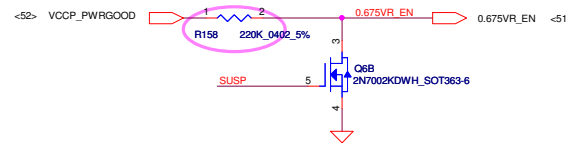
# **+3VALW TO +3VS** **+5VALW TO +5VS** **Load Switch**



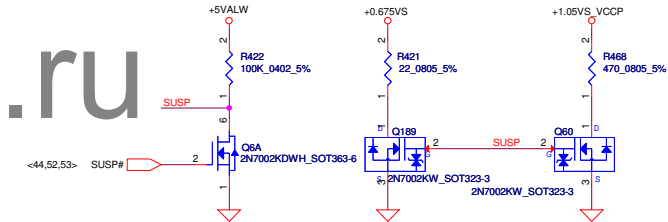
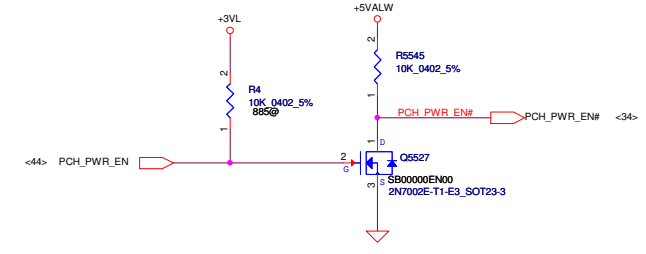
# **+3VALW TO +3V\_WLAN** **for AOAC and WOWL**



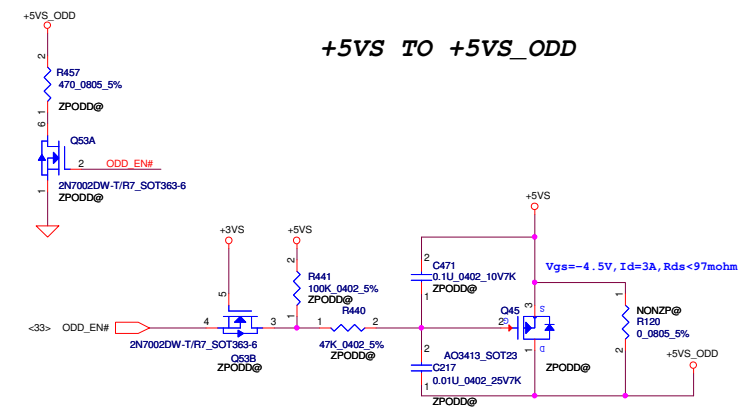
## **For S3 CPU Power Saving**



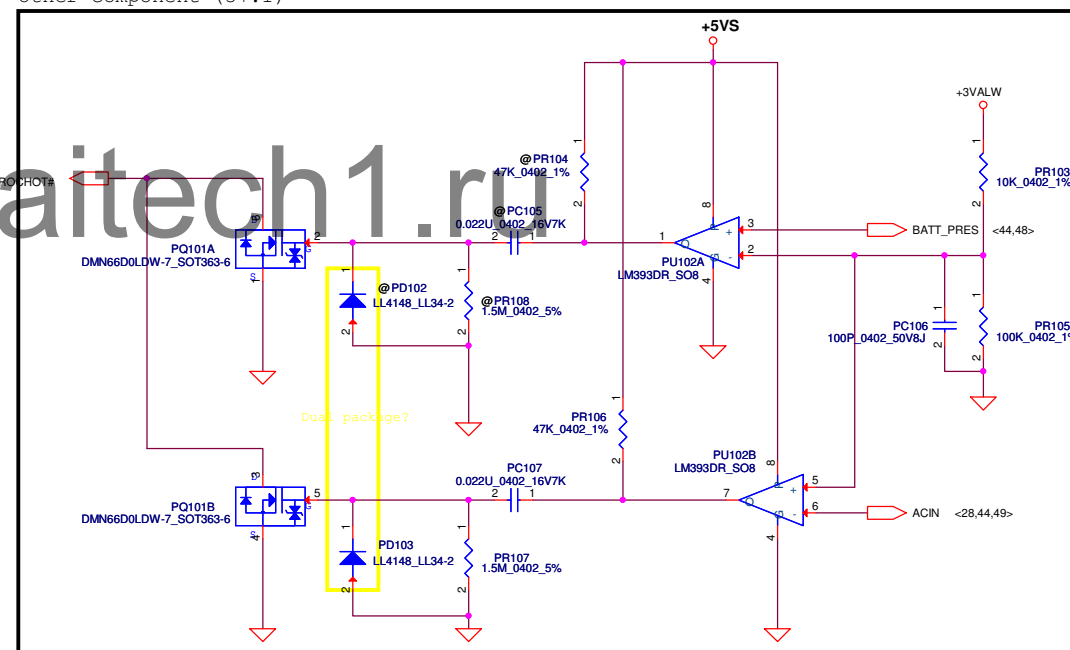
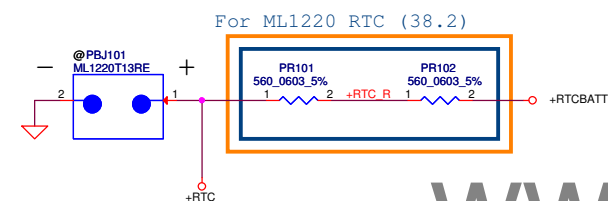
Reserve CAP to avoid Power Noise



## **+5VS TO +5VS\_ODD**



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				Date	Thursday, May 09, 2013
				Sheet	46 of 57
				Rev	1.0



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				Document Number	VSKAA		
Date:				Sheet	47	of	57



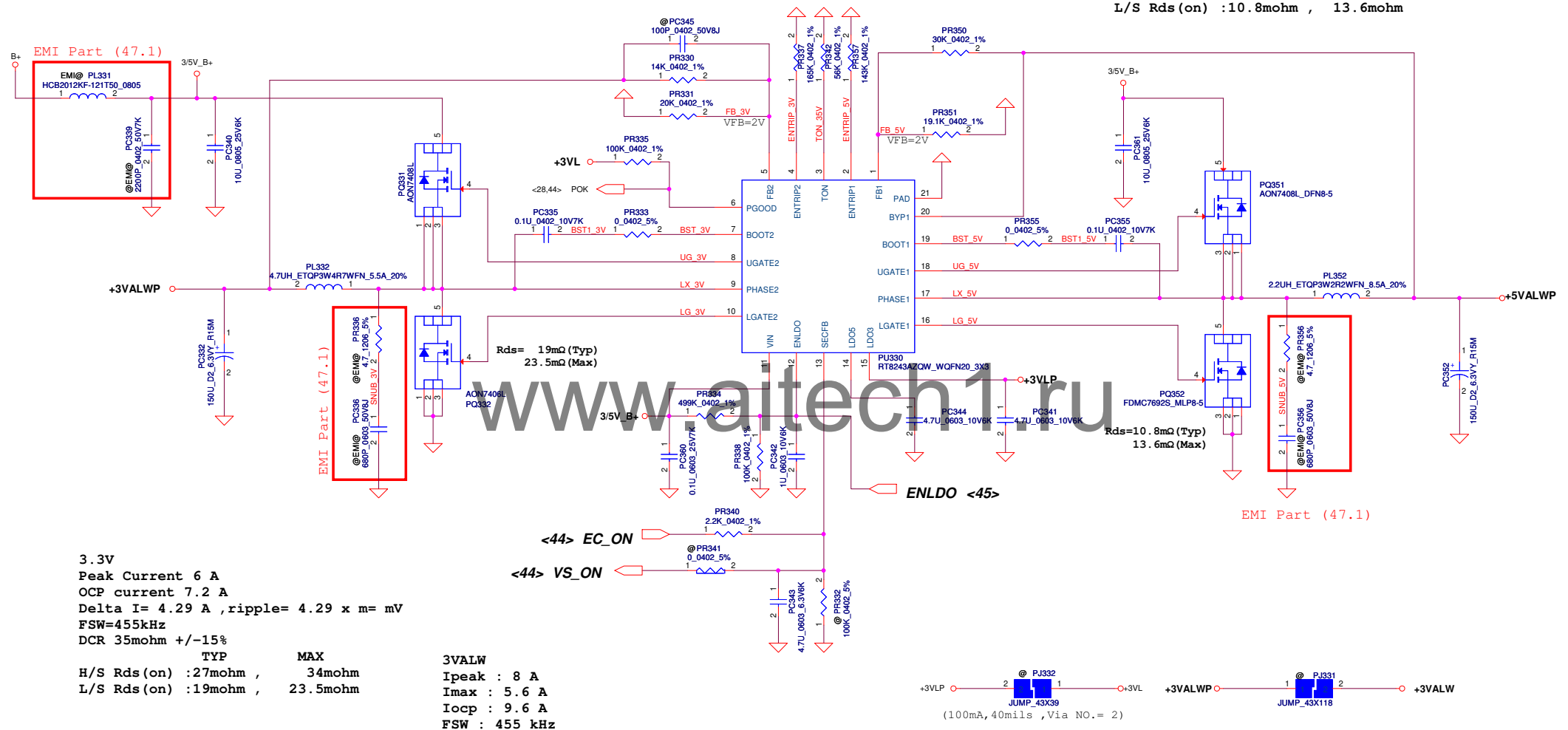
Charger controller (40.1), Support component (40.2)



3/5VALW controller (35.1), Support component (35.2)

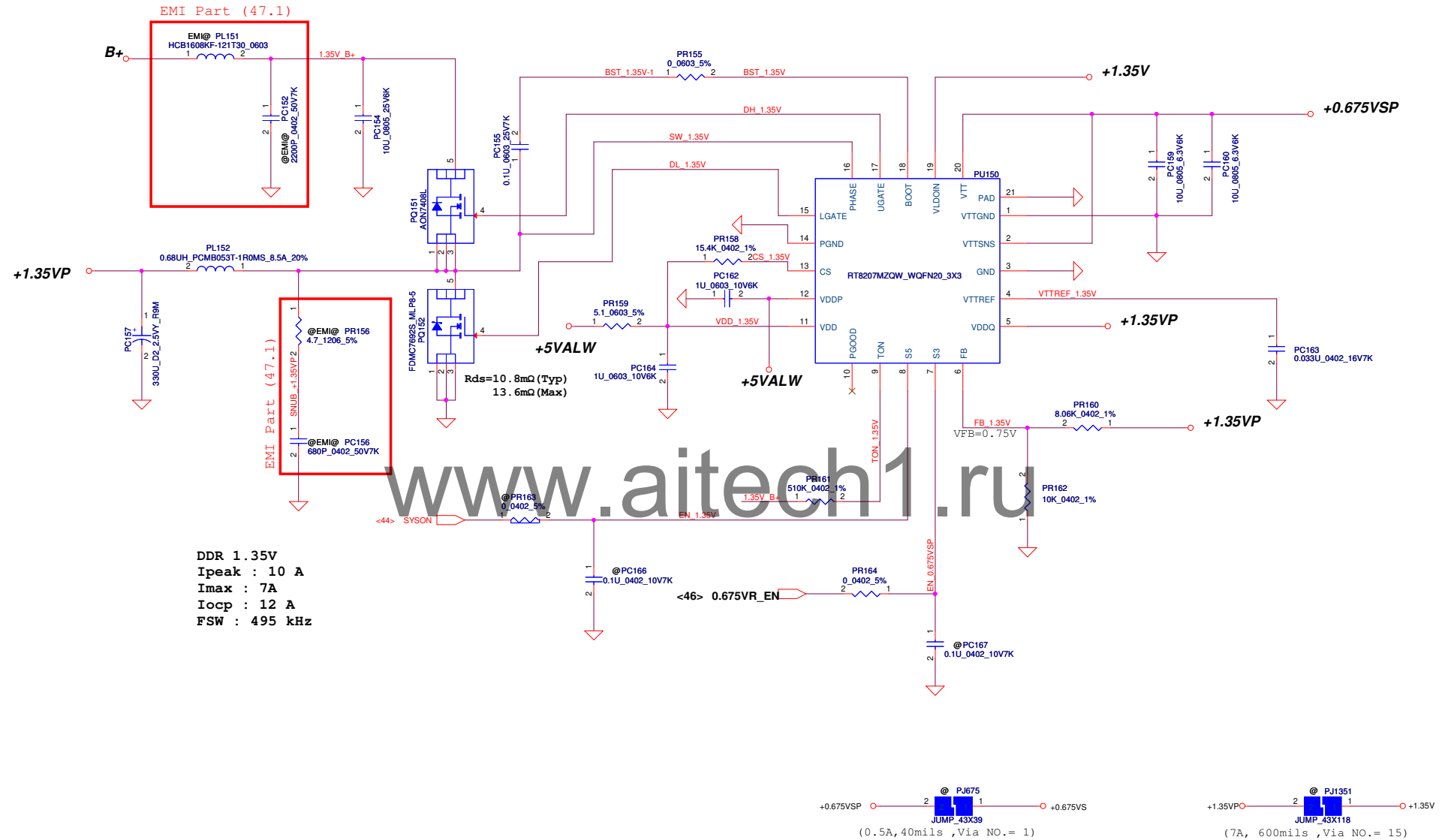
5VALW  
Ipeak : 12.5 A  
Imax : 8.75 A  
Iocp : 15 A  
FSW : 390 kHz

5V  
Peak Current 10 A  
OCP current 12 A  
FSW=390kHz  
Delta I= 1.28 A, ripple V = 1.28 \* 25 m= 32 mV  
DCR 13.2mohm +/-5%  
TYP MAX  
H/S Rds(on) : 27mohm , 34mohm  
L/S Rds(on) : 10.8mohm , 13.6mohm



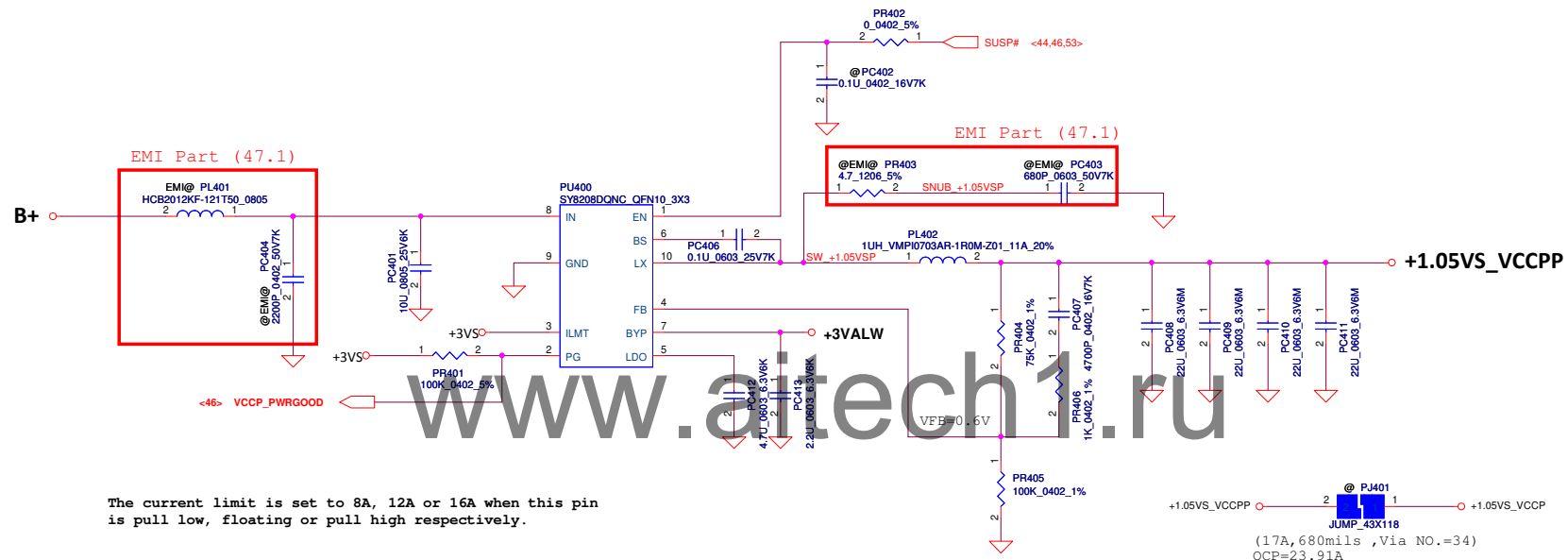
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title			
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				Rev 1.0			

## DDR controller (35.3), Support component (35.4)



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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	1.35VP/0.675VSP	
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				Custom	VSKAA	1.0
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1.05VCCP controller (35.5), Support component (35.6)



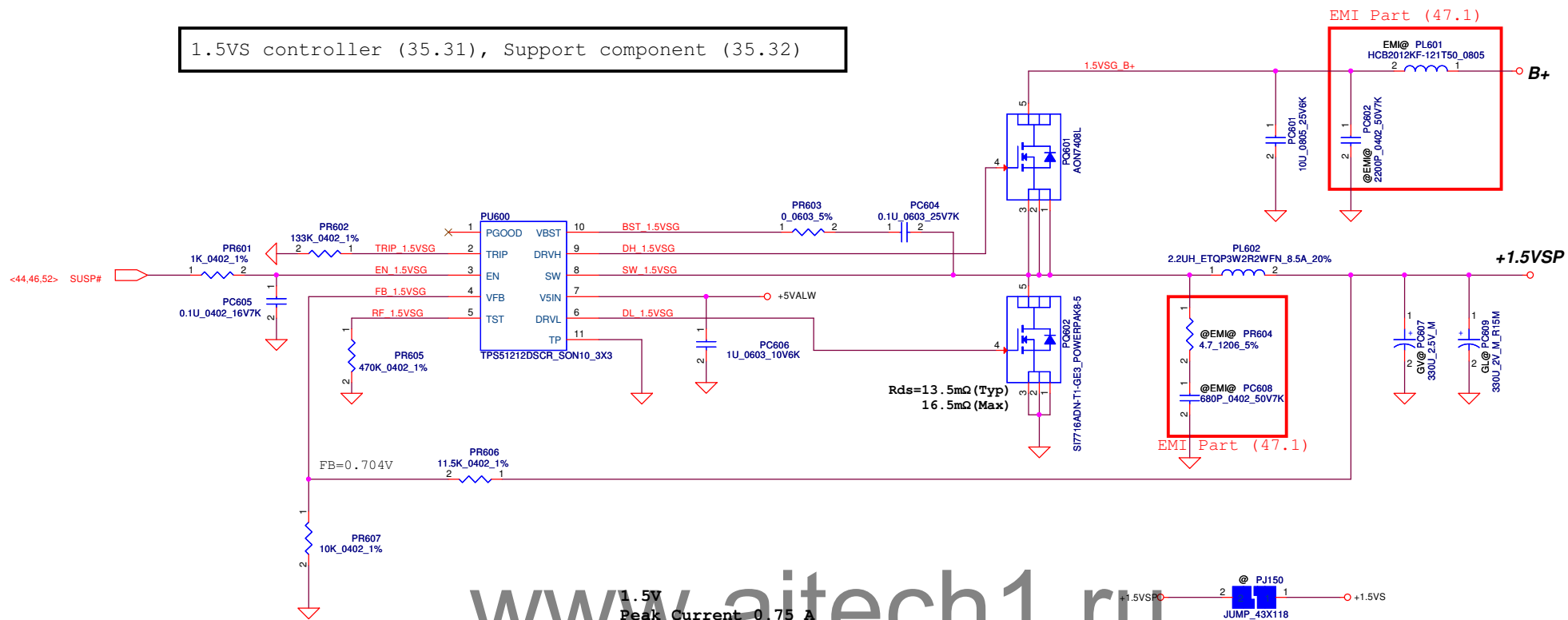
The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

1.05V  
Peak Current 11.35 A  
OCP current 16 A  
FSW=800kHz  
Delta I= 1.24 A, Rippe= x m= mV  
DCR 8.3~10 mohm  
TYP MAX  
H/S Rds(on) :22 mohm , mohm  
L/S Rds(on) :11 mohm , mohm

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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title
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1.5VS controller (35.31), Support component (35.32)



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1.5V  
Peak Current 0.75 A  
OCP current 0.95 A  
FSW= 290 kHz  
Delta I= A, Rippe= x m= mV  
DCR 8.3~10 mohm

TYP MAX  
H/S Rds(on) : 27 mohm , 34 mohm  
L/S Rds(on) : 13.5 mohm , 16.5 mohm

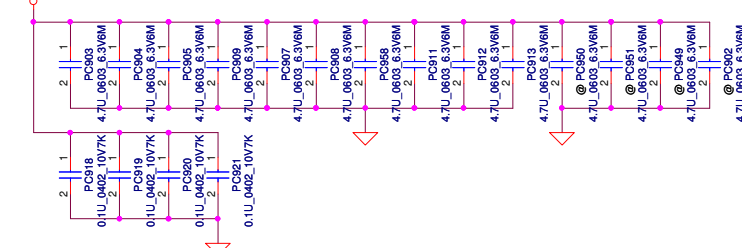
@ PJ150  
JUMP\_43X118  
15A, 600mils , Via NO.= 30)  
OCP=18A

TPS51212 for DIS SKU  
APL5930 for UMA SKU  
Confirm with HW for sequence control

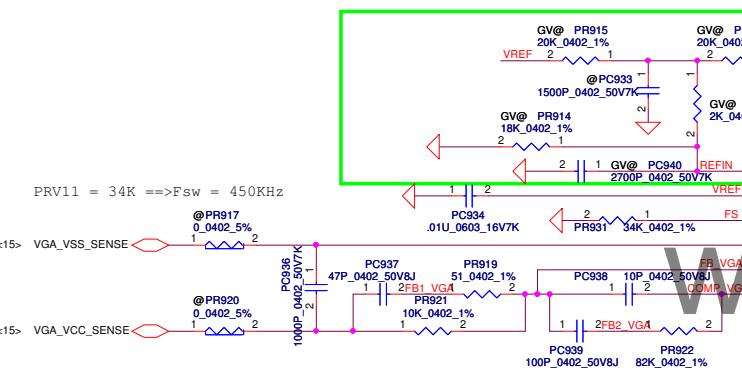
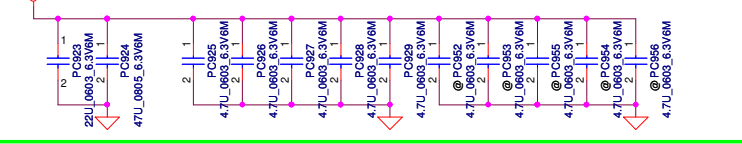
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/07/10		Deciphered Date		2013/07/10		Title	
										+1.5VS	
										VSKAA	
										Rev	
										1.0	
										Date	
										Thursday, May 09, 2013	
										Sheet	
										53 of 57	



**+VGA\_CORE Under VGA Core GB4-128 package**



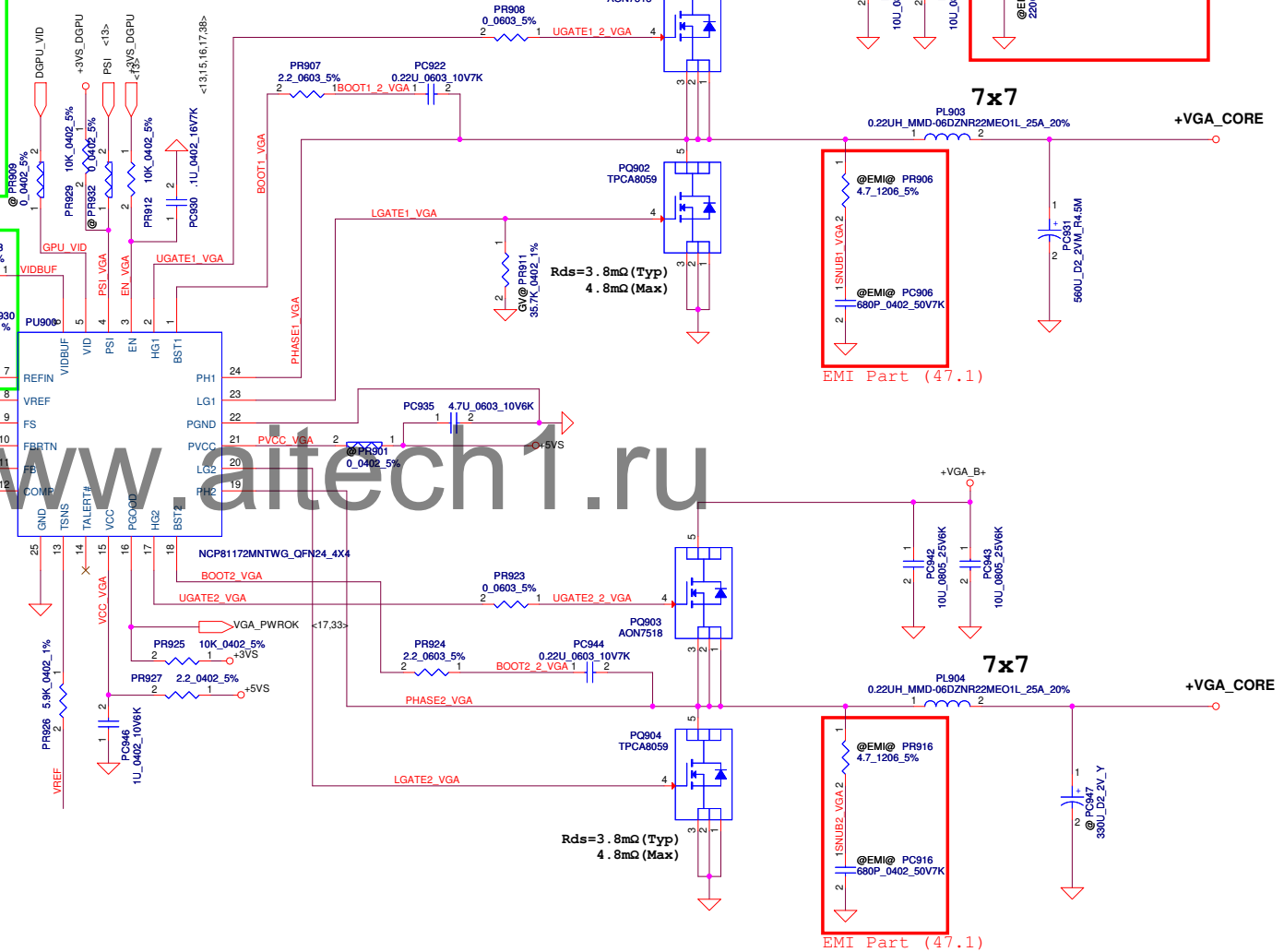
**+VGA\_CORE Near VGA Core**



	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	27 Kohm
C PC940	2.7 nF	1.8 nF

- GL@ PR913 39K\_0402\_1%
- GL@ PR915 30K\_0402\_1%
- GL@ PR930 3K\_0402\_1%
- GL@ PR914 27K\_0402\_1%
- GL@ PC940 1800P\_0402\_50V7K

VGA\_CORE controller (43.1), Support component (43.2)



# PWR PIR (Product Improve Record)

## VSKAA LA-9866P Schematic Change List

Item	Time (When)	Page (Where)	Location / Discription ( How / What)	Request (Who)	Reson (Why)
1	EVT--2012/10/24	P48-PWR-BATTERY CONN/OTP	@ PD5 / Remove ESD diode	COMPANY	For part count reduction
2	EVT--2012/10/24	P48-PWR-BATTERY CONN/OTP	@ PD6 / Remove ESD diode	COMPANY	For part count reduction
3	EVT--2012/10/24	P49-PWR-CHARGER	@ PC221 / Remove 10uF capacitor	COMPANY	For part count reduction
4	EVT--2012/10/24	P50-PWR-3VALW/5VALW	PC331,@PC332 / PC331 Reserve & PC332 Mount	ME	ME limitation
5	EVT--2012/10/24	P51-PWR-1.35VP/0.675VSP	@ PJ675 / JUMP_43x79 change to JUMP_43x39	PWR	For design change
6	EVT--2012/10/24	P51-PWR-1.35VP/0.675VSP	@ PJ1352 / Remove	PWR	For design change
7	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	PR541 / 475K change to 169K	PWR	For TP551631 under-shoot setting
8	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	@ PR553 / Remove (PWM3 floating)	COMPANY	For part count reduction
9	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	@ PC537 / Add 0402 Cap footprint	PWR	For TP551631 thermal setting
10	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	@ PC538 / Add 0402 Cap footprint	PWR	For TP551631 thermal setting
11	EVT--2012/10/24	P55-PWR-GPU_CORE	PR929 / Add 10K resistor	HW	Pull high PSI port
12	EVT--2012/10/24	P55-PWR-GPU_CORE	PR913 / 39K change to 20K(GV@)	PWR	For N14 PWM VID setting
13	EVT--2012/10/24	P55-PWR-GPU_CORE	PR915 / 39K change to 20K(GV@), 30K(GL@)	PWR	For N14 PWM VID setting
14	EVT--2012/10/24	P55-PWR-GPU_CORE	PR930 / 1.5K change to 2K(GV@), 3K(GL@)	PWR	For N14 PWM VID setting
15	EVT--2012/10/24	P55-PWR-GPU_CORE	PR914 / 30K change to 18K(GV@), 24K(GL@)	PWR	For N14 PWM VID setting
16	EVT--2012/10/24	P55-PWR-GPU_CORE	PR904 / 1.5K change to 0(GV@), 3K(GL@)	PWR	For N14 PWM VID setting
17	EVT--2012/10/24	P55-PWR-GPU_CORE	PC940 / Add 2.7nF(GV@), 1.8nF(GL@)	PWR	For N14 PWM VID setting
18	EVT--2012/10/24	P55-PWR-GPU_CORE	PC933 / Reserve	PWR	For N14 PWM VID setting
19	EVT--2012/10/24	P50-PWR-3VALW/5VALW	PR337 / 235K change to 165K	PWR	For RT8243 3V OCP setting
20	EVT--2012/10/24	P50-PWR-3VALW/5VALW	PR357 / 156K change to 143K	PWR	For RT8243 5V OCP setting
21	EVT--2012/10/24	P51-PWR-1.35VP/0.675VSP	PR158 / 16.2K change to 15.4K	PWR	For RT8208 1.35V OCP setting
22	EVT--2012/10/24	P55-PWR-GPU_CORE	PR931 / 71.5K change to 34K	PWR	For NCP81172 Fsw setting
23	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	PC521 / Add 1000P_0402 Capacitor	PWR	For design change
24	EVT--2012/10/24	P54-PWR-CPU_CORE-37W	PC533 / Add 1000P_0402 Capacitor	PWR	For design change
25	EVT--2012/10/24	P55-PWR-GPU_CORE	PR927 / change resistor PN	PWR	For PN setting error
26	DVT--2012/12/07	P48-PWR-BATTERY CONN/OTP	PF2 / change component for cost down	COMPANY	For cost down
27	DVT--2012/12/07	P49-PWR-CHARGER	PQ203 / AON6504 Change to TPCA8057	PWR	For design issue
28	DVT--2012/12/07	P50-PWR-3VALW/5VALW	PC351, PC352 / Remove OSCON mount polymer CAP	ME	ME limitation
29	DVT--2012/12/07	P50-PWR-3VALW/5VALW	PR409 / Add 100K	PWR	Pull high for PG00D port
30	DVT--2012/12/07	P50-PWR-3VALW/5VALW	PC341, PC344 / Add 4.7u for LDO5 & Change PC341 size to 0603	PWR	for IC default setting
31	DVT--2012/12/07	P51-PWR-1.35VP/0.675VSP	PL152 / Change choke value	PWR	Common design change
32	DVT--2012/12/07	P52-1.05VS_VCCP	PL401 / Change bead	PWR	Common design change
33	DVT--2012/12/07	P52-1.05VS_VCCP	PR403, PC403 / Reserve PR403 & PC403		
34	DVT--2012/12/07	P54-PWR-CPU_CORE-37W	PL502, PL505 / Change choke value	PWR	Common design change
35	DVT--2012/12/07	P54-PWR-CPU_CORE-37W	PC528, PC529, PC537, PC538 / Add 0402 Cap footprint	PWR	Common design change
36	DVT--2012/12/07	P55-PWR-GPU_CORE	PC993, PC994, PC995, PC996, PC997, PC1101, PC1103 / Add MLCC PC993~PC997, remove polymer PC1101, PC1103	PWR	For HF design
37	DVT--2012/12/07	P55-PWR-GPU_CORE	PC934 /	PWR	Common design change
38	DVT--2012/12/07	P55-PWR-GPU_CORE	PL903, PL904 / Change vendor	PWR	Change for losing
39	DVT--2012/12/07	P55-PWR-GPU_CORE	PR912 / Change short pad to 10K	PWR	Pull high for EN port
40	DVT--2012/12/07	P52-1.05VS_VCCP	PC407 /	PWR	Common design change
41	PVT--2013/02/25	P54-PWR-CPU_CORE-37W	PR541 change from 169K to 64.9K PR542 change from 150K to 20K PR547 change from 174K to 196K PC514 reserve PR532 change from 3.16K to 3.24K PR554, PR562 change from 2.37K to 2.26K PR555, PR563 change from 17.8K to 18.7K	PWR	for IC TP551631 edition change from ES1.1 to ES2.1 fine tune
42	PVT--2013/03/04	P55-PWR-VGA_CORE	PR904, PR918, PR928, PC945 remove PR914 change from 24K to 27K	PWR	Remove and change for Richtek solution setting
43	PVT--2013/03/04	P52-1.05VS_VCCP	PR406 add 1K PC407 change from 330p to 4700p	PWR	Common design change
44	PVT-2013/03/21	P55-PWR-VGA_CORE	PR911 mount	PWR	Mount for GV2 setting
45	PVT-2013/03/21	P55-PWR-VGA_CORE	PC947 reserve	PWR	For part count reduction
46	PVT-2013/03/21	P53-PWR-1.5VS	PR602 change to 133K	PWR	adjust current lim it value
47	PVT-2013/03/21	P52-PWR-1.05VS_VCCP	add PR406	PWR	circuit protection function
48	PVT-2013/03/21	P51-PWR-1.35VP/0.675VSP	change PL152 part number	PWR	for design change

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# HW PIR (Product Improve Record)

VSKAA LA-9866P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2

GERBER-OUT DATE: 2012/12/05

NO DATE PAGE MODIFICATION LIST

PURPOSE

Item	Date	Page	Action	Component	Request
1)	11/19	24	Delete	R23,R24,R25,R26	HDMI Redriver SMBus connect to EC directly
2)	11/19	31	Change Config	RH17 to LVDS@	
3)	11/19	31	Change Config	RH18 to IEDP@	
4)	11/19	44	Change	RB36 from 2.2K to 0 ohm	Change EC_ON workaround to power side
5)	11/19	44	Change Config	CB50 to @	
6)	11/19	42	Change Config	CA32 to always mount	
7)	11/19	30	Change	PCH_SPICS1# to UH3, PCH_SPICS0# to UH4	For Shark Bay ME code location
8)	11/19	44	Change	EC pin128 from EC_CS0# to EC_CS1#	For SW request
9)	11/22	33	Change	PCH_GPIO69 to PROJECT_ID	For SW request
10)	11/22	33	Change	PCH_GPIO22 to VRAM_DR_SR#	For VBIOS setting of DRANK or SRANK
11)	11/23	26	Change Config	C238~C243 to CRT@EMI@	
12)	11/23	23	Add	D92	For isolate the +3VL power rail form LID_SW#
13)	11/28	41	Change	Change C987,C900 from 1206 to 0805	To avoid MLCC from cracking
14)	11/29	23	Change	Change JLVDS.4 from LID_SW# to BK_OFF#	Common design change
15)	11/29	43	Change	Change JSPK from 8 pins to 6 pins	Common design change
16)	11/29	33	Change	Delete SPK_DET1 and change SPK_DET0 netname to SPK_DET	SPK detection method was changed
17)	11/29	42	Change	Change RA50 to 269@	Used for avoiding from S&M noise issue
18)	11/29	12	Change	Change CD31 from 1206 to 0805	To avoid MLCC from cracking
19)	11/29	24	Change	Stuff 8401@ as default add reserve R168,R169	For the purpose of HDMI 4K2K jetter cleaner
20)	11/29	40	Add	Add QW1,RW3,RW4 to have inversion circuit	For normal close connector type
21)	11/29	45	Add	Add H19, change H7 to H_4P0,change H4,H5 to H_3P3	ME's requirement
22)	12/02	26	Add	Add R62 R63 22ohm	For CRT undershoot issue
23)	12/02	44	Change	Change PM_SLP_S4# from pin127 to pin84	For EC fix code design
24)	12/02	44	Change	Change USB_EN#0 from pin84 to pin23	For EC fix code design
25)	12/02	44	Change	Change FB_CLAMP from pin23 to pin127	For EC fix code design
26)	12/03	05	Add	Add CC63,CC68,CC69,CC83 100P	For ESD
27)	12/03	31	Change	Change CH104 to 0.1u	For ESD
28)	12/03	10	Change	Change CC53 to 47u	For cost down
29)	12/03	41	Add	Add QR1,RR1,RR2,RR3,RR4	For colay 14640 Charge IC

===== PVT Modify Items =====

1)	02/03	05	Del	Del C6 (1000P on +FAN1)	
2)	02/03	11	Change	Change RC78 to 1K	For SM_DRAMRST# rising smoothly
3)	02/03	11	Del	Del CD15,CD2,CD22,CD23,CD12	For cost down
4)	02/03	12	Del	Del CD28,CD46,CD43,CD44,CD38	For cost down
5)	02/03	12	Change	RC109,RC110,RC111,RC120,RC121,RC122 from 0.5% to 1%	For cost down
6)	02/03	12	Reserve	CC65,CC71,CC72,RC3,RC8,RC9	For common design
7)	02/03	17	Del	CV58	For part count
8)	02/03	25	Del	C264	For part count
9)	02/03	25	Change	U16 to SA00006H000	For common design
10)	03/08	23	Reserve	D89	For ESD request
11)	03/15	44	Reserve	CB17, CB18, CB19	For ESD request
12)	03/15	05	Reserve	CC2,CC3	For ESD request
13)	03/15	33	Reserve	CH7	For ESD request
14)	03/15	23	Add	D2, D3 on INT_MIC_DATA & INT_MIC_CLK	For ESD request
15)	03/15	40	Add	CW10~CW14, LW1~LW6	For solving EMI test fail
16)	03/15	23	Reserve	R104, R105	For colay EMI common mode choke
17)	03/15	26	Change	R138 to 150ohm array chip resistor	For part count reduce
18)	03/15	45	Add	R268,R269	For WOWL LED behavior requested by customer
19)	03/15	42	Change	RA42 from 0 ohm to bead	For EMI request
20)	03/15	44	Add	RB17, RB38	For solving bobo noise
21)	03/15	44	Add	RB14 & link EC pin 123 to POK	For power request
22)	03/15	11	Change	RC78 from 0 ohm to 1K	For making SM_DRAMRST# rising more better
23)	03/15	31	Add	RH127, RH128	For HDMI_HPD no use port to default pull down
24)	03/15	35	Change	RH14 to short pad & reserve RH15 to ohm	For change +VCCCFUSE to +1.05VS_PCH
25)	03/15	31	Change	RH155 to 150ohm array chip resistor	For part count reduce
26)	03/15	25	Change	U16 from AP2330 to AP2151	For common design
27)	03/15	30	Change	4M+2M solution to 8M only solution	For common design
28)	03/15	25	Del	C264	For part count reduce
29)	03/15	17	Del	CV58	For part count reduce
30)	03/15	22	Del	LT3	For no colay RTD2132S
31)	03/15	23	Del	R81, R82	For no colay RTD2132S
32)	03/15	40	Change	CW9 from 10P to 4.7P	For ME limitation
33)	03/15	45	Del	SW3	For ME limitation

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				Custom		1.0	
				Date		Thursday, May 09, 2013	
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